
TECHNICAL DECISION MAKER PRESENTATION

Cisco Catalyst 9500 Series

Prepared as a convenient PDF reference for network planning, platform evaluation, and procurement discussions.

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Cisco Catalyst 9500 Series

Technical Decision Maker Presentation

August 26, 2026

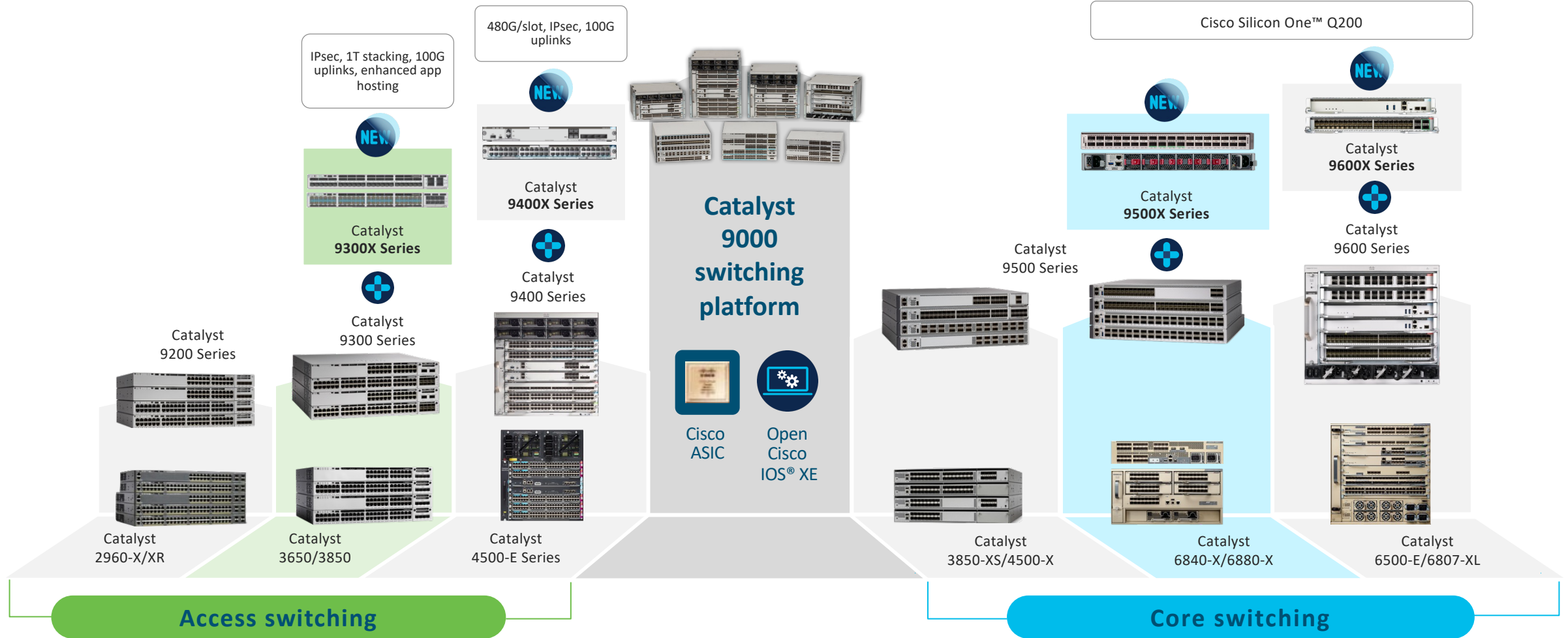
Agenda

- Hardware
- Power and Env
- Architecture
- User Centric Platform design
- SDM templates
- Cisco® UADP 3.0 ASIC
- Cisco® Silicon One ASIC
- Platform Comparison
- C9500 App Hosting
- Competitive Info
- High Availability
- Security Overview
- Software Features
- Catalyst 9000 Design
- Intent-based Networking
- Closing

Hardware

Catalyst 9000X – Expanding industry leadership

Adding the “X factor” to the industry’s leading switching family



Cisco Catalyst 9500 Series

Purpose-built fixed core/aggregation switches

UADP 2.0



UADP 3.0



Silicon One Q200

- 40G at the price of 10G
- Industry's first 40G enterprise switch
- Optimized 10G switch for midsize backbone

- Up-to 48 25 GE Ports
- Industry's first 100G enterprise switch
- Flexible templates

- Reversible Bi-directional Airflow
- Ultra Deep 8GB Buffers
- High route scale (2M) and Mac scale (256K)



Modular fans



Modular uplinks



Modular power supplies



Storage for application hosting

Catalyst® 9500X - Extending Cisco® Catalyst® 4500-X and 6800 Series leadership in fixed core

Upto 26x throughput (6 Tbps)

Upto 48x performance (8 Bpps)

No oversubscription

8x 400GE Density

Pluggable SSD storage

USB 3.0

8x memory and 4x flash

8 core CPU

Customizable templates

Cisco StackWise® Virtual*

*Supported on 9500 and 9500H. Roadmap for 9500X

Cisco Catalyst 9500X

Addressing the Campus Core + Edge Market

More than just “Speeds & Feeds”



System Capacity

- **Higher Port Speeds**
enabling newer Ethernet speeds and types, such as 50G SFP and 400G QSFP
- **More Access Bandwidth**
higher density of 802.11ac moving to 11ax, HD Video (1080p) moving to UHD (4K)
- **Non-Blocking**
Core needs non-blocking (1:1) performance



System Scale

- **High-Scale Routing**
support for full IPv4 and IPv6 Internet + LAN + VRF routing
- **Flexible Transport Options**
support for MPLS-VPN, SD-Access and BGP-EVPN with 4K VRFs
- **Centralized Wireless**
support for high MAC and ARP/NDP scale



Port Density

- **More Uplinks**
support for multiple QSFP uplinks, with LR/ZR optics for redundant edge connections
- **More Downlinks**
support for hundreds of SFP ports/breakouts
- **Port Options**
mix of SFP & QSFP ports, at various interface speeds

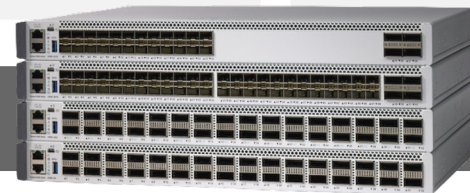


Flexibility

- **Programmable ASIC**
Enable new features and encapsulations
- **Model-driven Microcode**
hardware functions use model-driven APIs
- **App Hosting Infrastructure**
support Docker applications
- **Architecture-level HA**
L2/L3 redundancy with Stackwise Virtual and GIR



Core + Edge



Core + Distro



Cisco Silicon One™



Switching Silicon

- **High Throughput**
extremely fast hardware-based L2-L4 forwarding and services (measured in Terabits per second)
- **Optimized Scale**
optimized for Campus LAN environments with moderate IP & MAC scale (10s-100s of thousands)
- **Low Latency**
extremely low hardware-based system latency (measured in Nanoseconds & Microseconds)
- **Streamlined Buffering**
shallow buffering systems to reduce latency, with very high throughput



Routing Silicon

- **Flexible Features**
complex, stateful L3-L7 forwarding and services (measured in Gigabits per second)
- **Massive Scale**
optimized for WAN/SP environments with very high IP scale (100s of thousands - millions)
- **Mixed Interfaces**
support for Ethernet, Serial, Cellular and other types and speeds in a single system
- **Deeper Buffering**
deep buffers to accommodate different speeds, bursts and different flow patterns

Cisco Silicon One Bringing Switching and Routing convergence

Cisco Silicon One™ Q200

Industry leading Switching and Routing Silicon



12.8T BW



8.1 Bpps



8G HBM for
deep buffers



10M IPv4
or 5M IPv6
route scale



Fully P4
Programmable
Pipeline



50G PAM4
Serdes

Cisco Silicon ONE Q200

Industry Leading 12.8T System on Chip



First 7nm ASIC providing lowest
watts/GE power consumption



Fully P4 programmable enabling
feature velocity



Multi slice architecture for
flexibility and scale

Routing Capabilities with Switching Power and Performance

Catalyst 9500X Family

Extending the Catalyst 9500 high-performance fixed core

Non-XL scale



Catalyst® 9500H
(UADP 3.0)



C9500-32C / C9500-32QC



C9500-48Y4C / C9500-24Y4C

Total capacity
3.2 Tbps
32x 100G or
48x 25G + 4x 100G

Core
+
Edge

XL scale



Catalyst 9500X
(Silicon One™ Q200)



C9500X-28C8D

IOS-XE 17.7.1



C9500X-60L4D

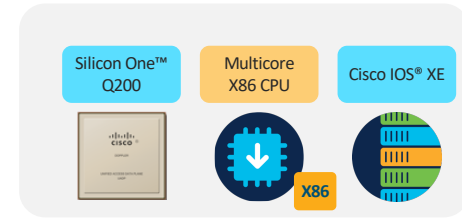
IOS-XE 17.10.1

~2X

Total capacity
6.0 Tbps
28x 100G + 8x 40/100/400G or
60 x 10/25/50G + 4 x 40/100/400G

Catalyst 9500X – Extending leadership in the core

Redefining the campus WAN edge



Industry first

2x switching performance

10x route scale and ultra-deep buffer

10x route scale and ultra-deep buffer

Up to 2 million route scale
8 GB of ultra-deep buffers

Industry first

Carrier-class QoS

2 levels of HQoS
VOQ architecture

Unmatched flexibility

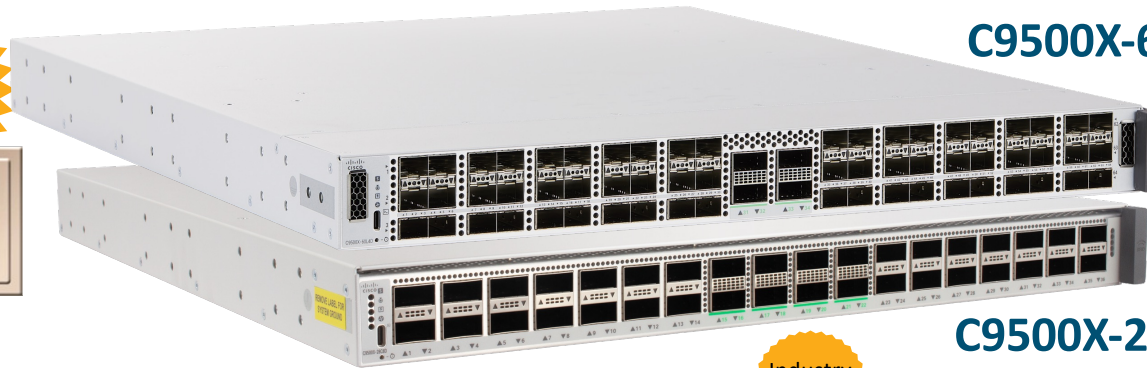
400G leadership

Secure

Application hosting

400G QSFP-DD

Powered by S1 Q200



C9500X-60L4D

C9500X-28C8D

Reversible airflow

Front to back
Back to front

Highest resiliency

Redundant fans (5+1)
Redundant power supplies
StackWise® Virtual*

Industry first

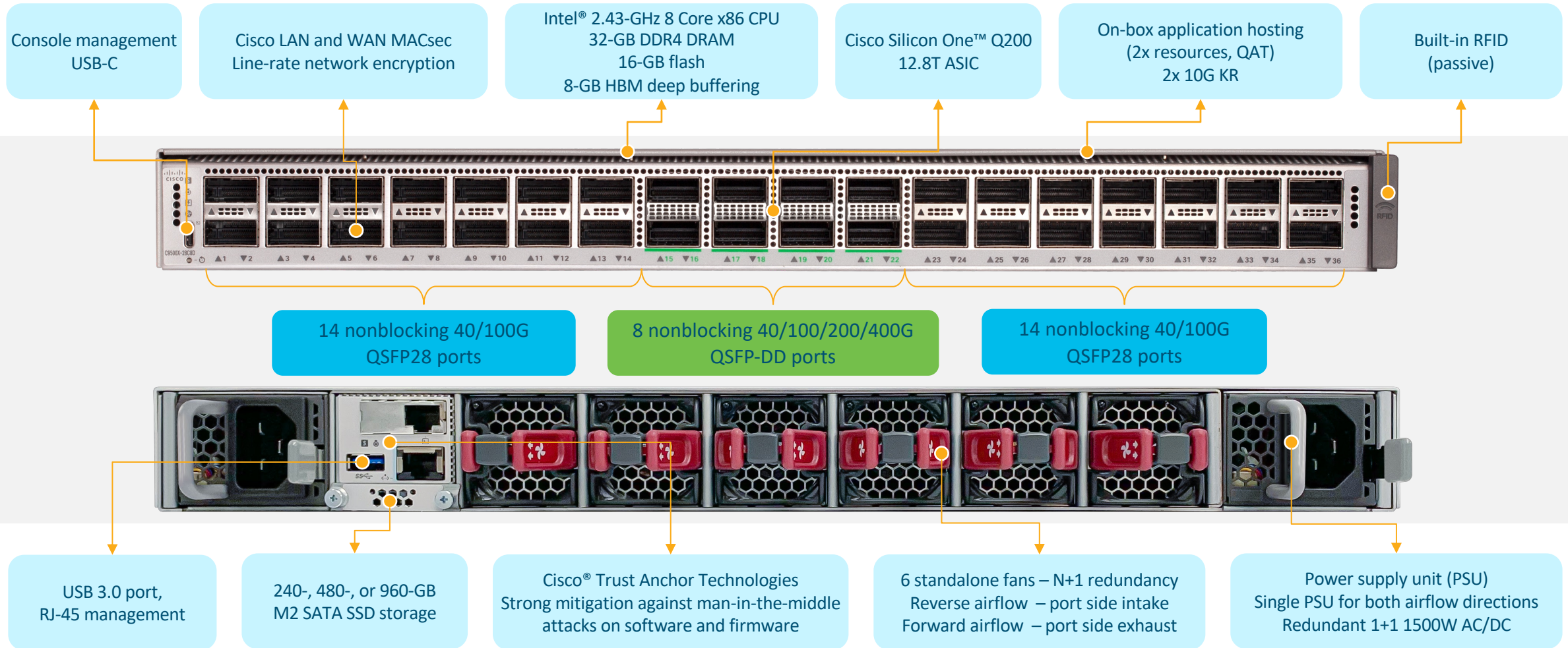
Enhanced encryption

LAN MACsec
WAN MACsec
IPSec^

*17.10.1 for C9500X-28C8D and 17.11.1 for C9500X-60L4D
^ Hardware capable – Only C9500X-60L4D

Cisco Catalyst C9500X-28C8D: line rate 6T of capacity

High-level overview



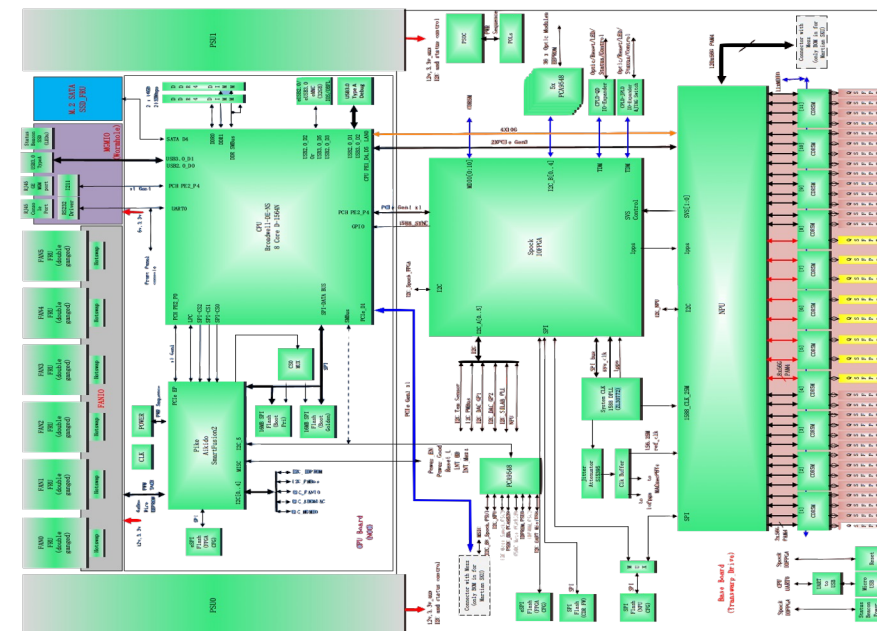
C9500X-28C8D

Gen 2 fixed 1RU QSFP switch: 36x 100G or 28x 100G + 8x 400G

6.0
Tbps

Target FCS
Q1CY22
Software
Cisco IOS® XE 17.7.1

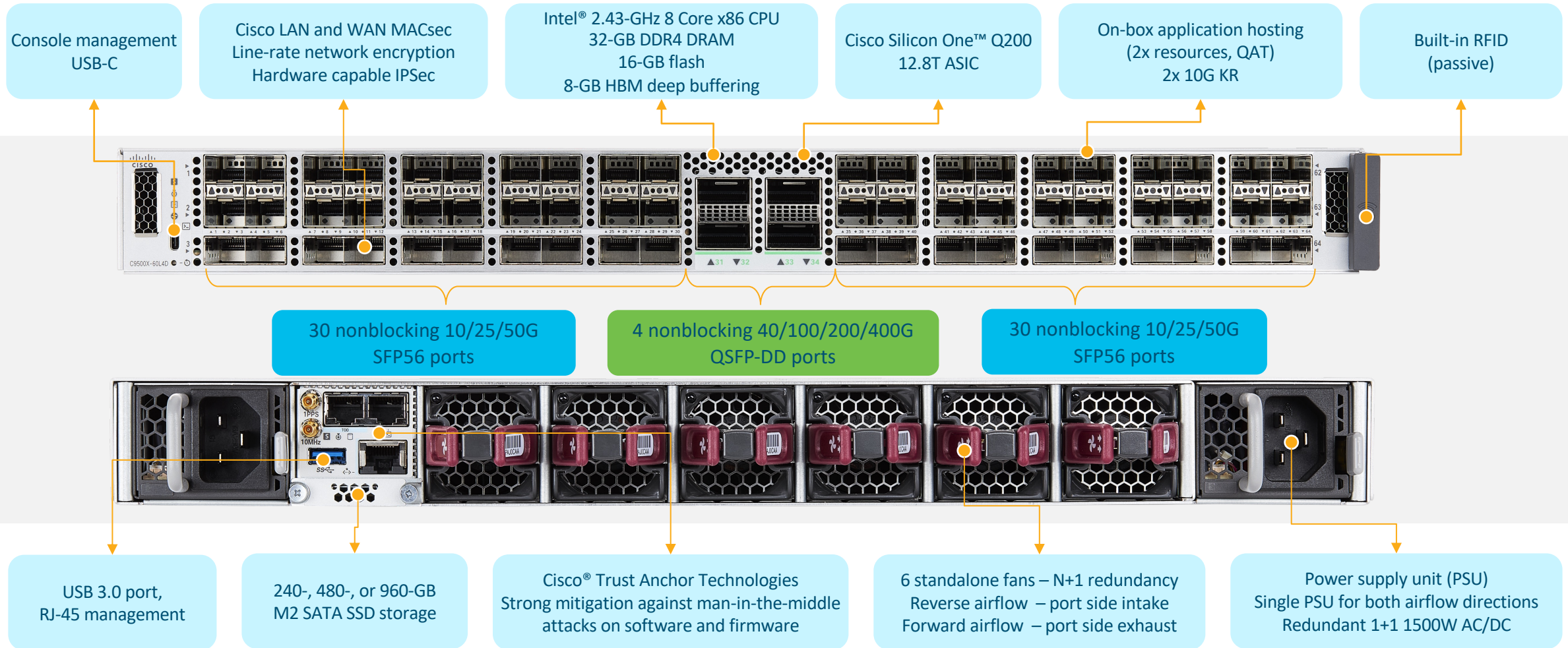
- 1x Cisco Silicon One™ Q200 ASIC
 - 6.0 Tbps system throughput
 - 28x QSFP28 ports - 40/100G
 - 8x QSFP-DD ports - 100/200*/400G
- 1x 8C 2.4-GHz x86 CPU with 2x 16-GB (32GB) DDR4 DRAM
- 16-GB flash; optional SSD (480 GB, 960 GB)
- 12x CDR5M PHYs
 - MACsec, WAN MACsec, ClearTag v3.4
 - IEEE 1588 and PTPv2*
- Various SFP breakout and QSA support*



*Hardware capable. Roadmap (not committed).

Cisco Catalyst C9500X-60L4D: line rate 4.6T of capacity

High-level overview



C9500X-60L4D

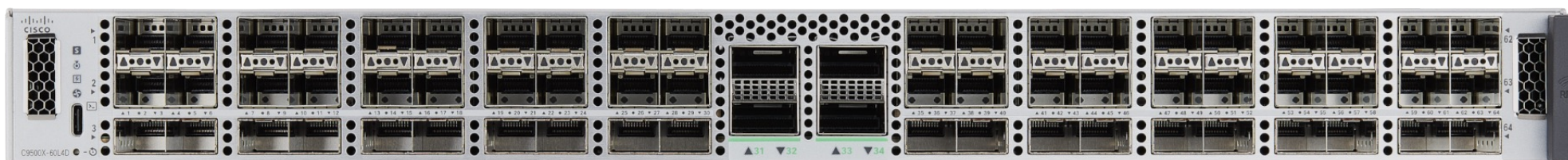
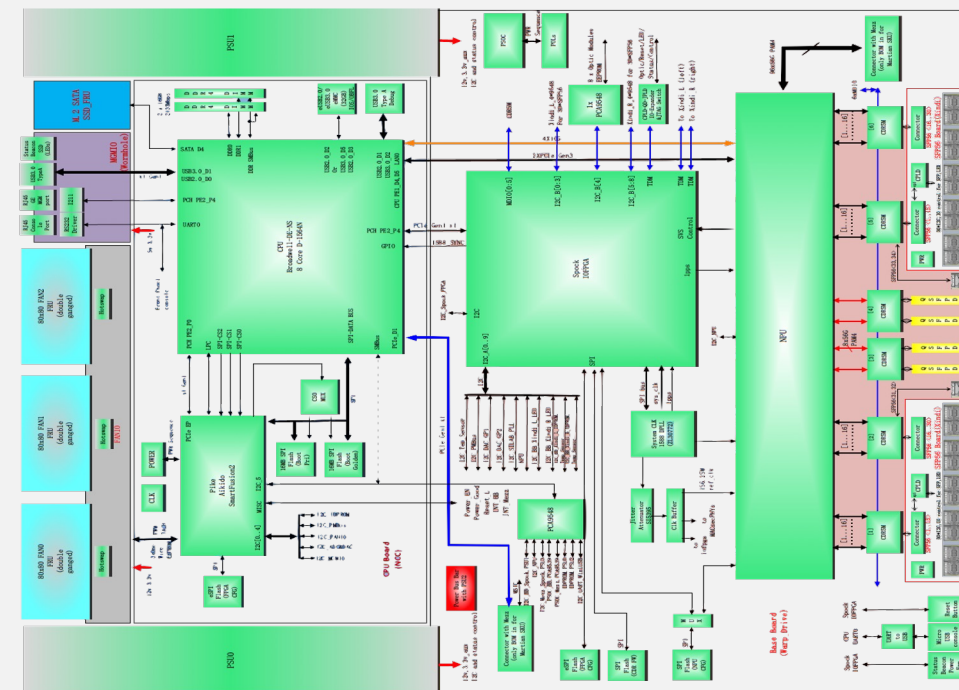
Gen2 Fixed - 1RU SFP + QSFP Switch

FCS: Jan 2023

Software:
IOS-XE 17.10.1

4.6
Tbps

- **4.6Tbps System Throughput**
 - 60x SFP56 ports, 10/25/50GE
 - 4x QSFPDD ports, 100/200/400GE
- **1x Cisco SiliconOne Q200 ASIC (12.8T)**
- **1x 8C 2.4GHz x86 CPU**
- **2x 16GB (32GB) DDR4 DRAM**
- **6x Mediatek 3723PQ CDR5M PHYs**
 - Ipsec*, MACSec, WAN-MACSec, ClearTag v3.4
 - IEEE 1588 & PTPv2*
- **Various SFP Breakout & QSA support (max 92*)**

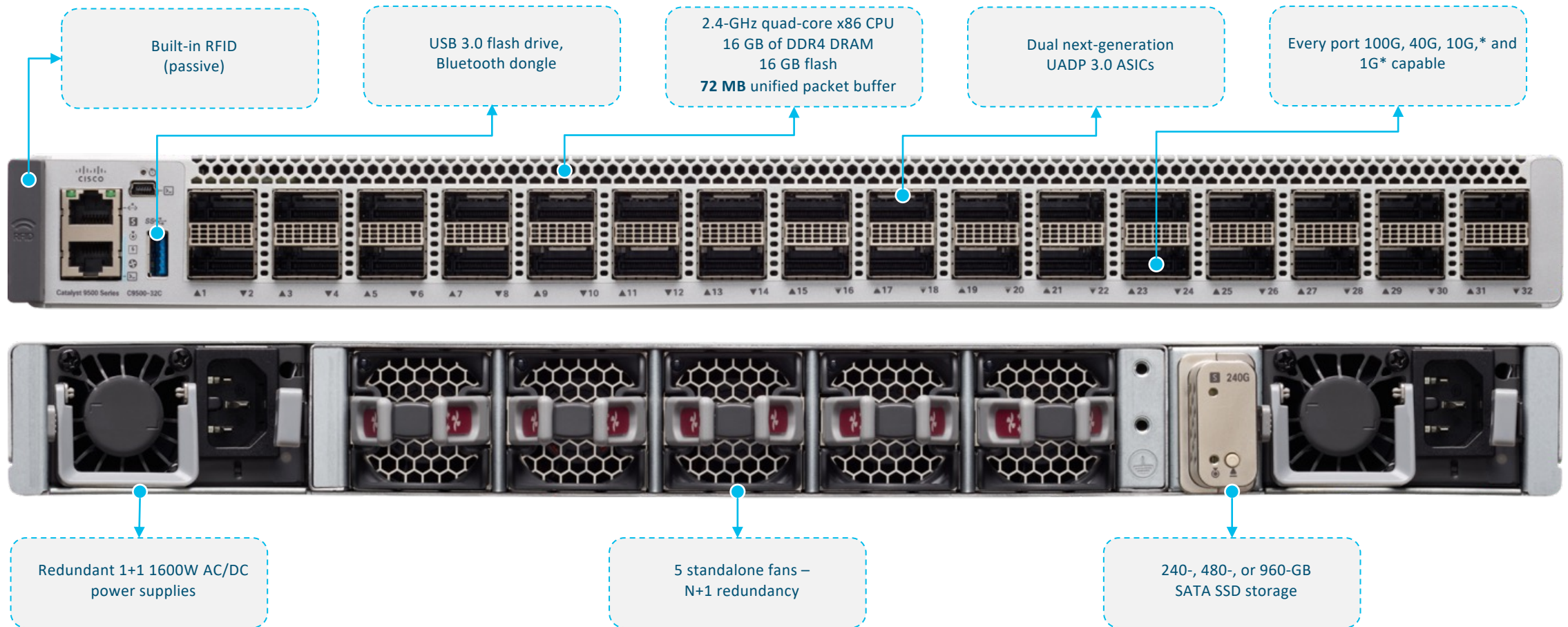


* SW Roadmap (FCS+)

Cisco Catalyst 9500 High Performance Series Switches

Cisco Catalyst 9500-32C

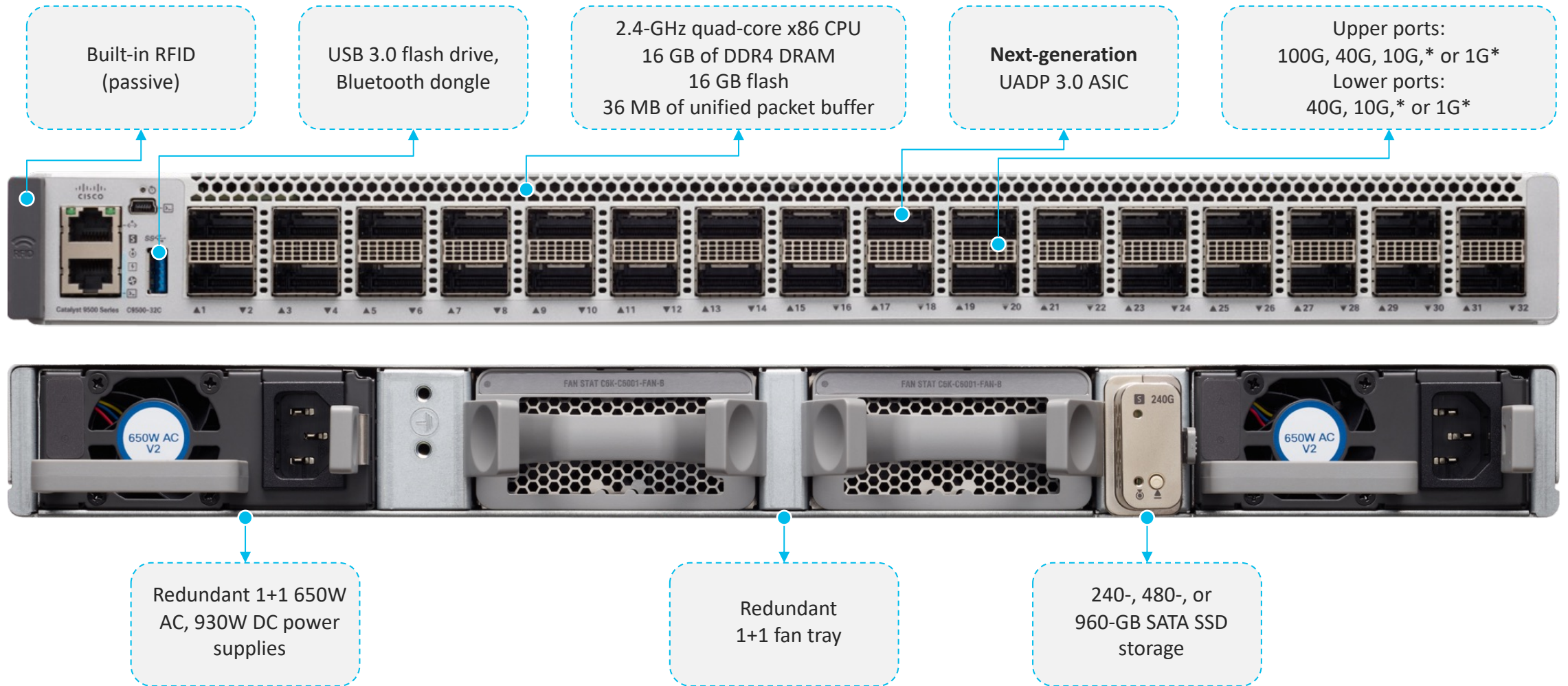
High-level overview



* With QSFP to SFP (QSA) adapter.

Cisco Catalyst 9500-32QC

High-level overview

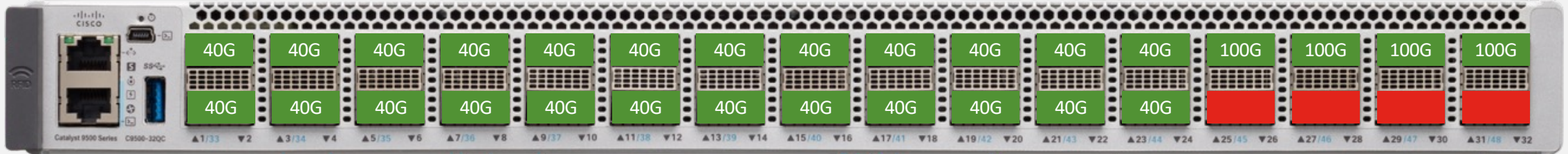


* With QSA adapter.

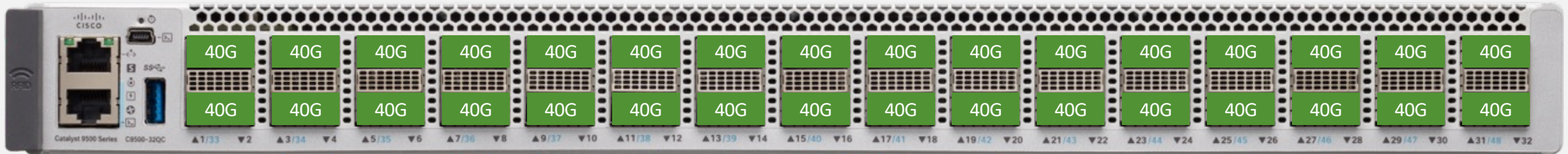
Cisco Catalyst 9500-32QC

Configuration modes

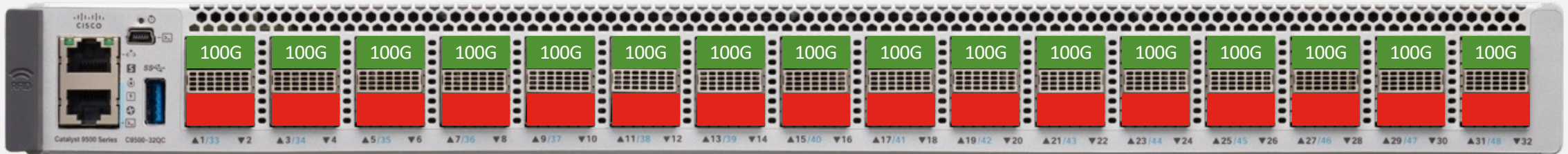
24 ports 40G + 4 ports 100G – default configuration



32 ports 40G



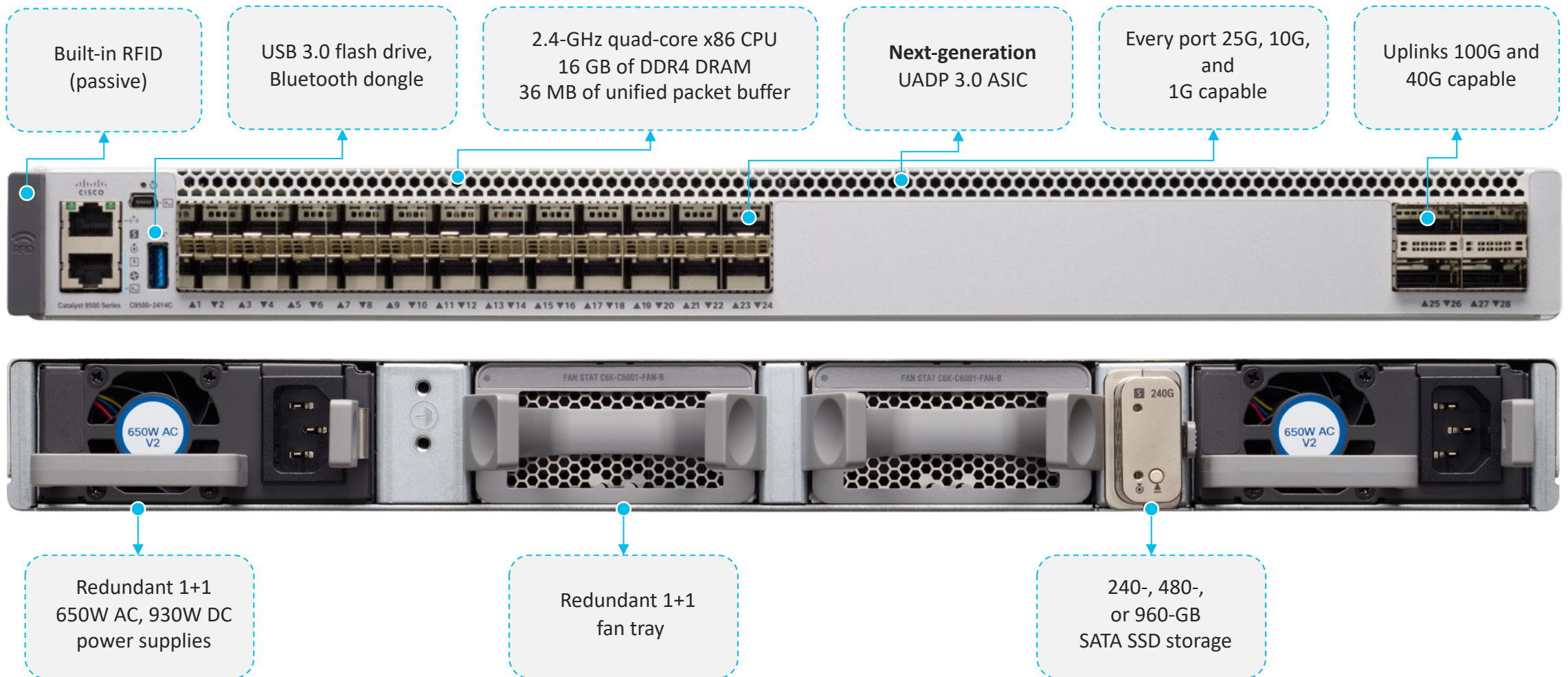
16 ports 100G



Note: Other configuration options are supported, including mix and match of speeds.

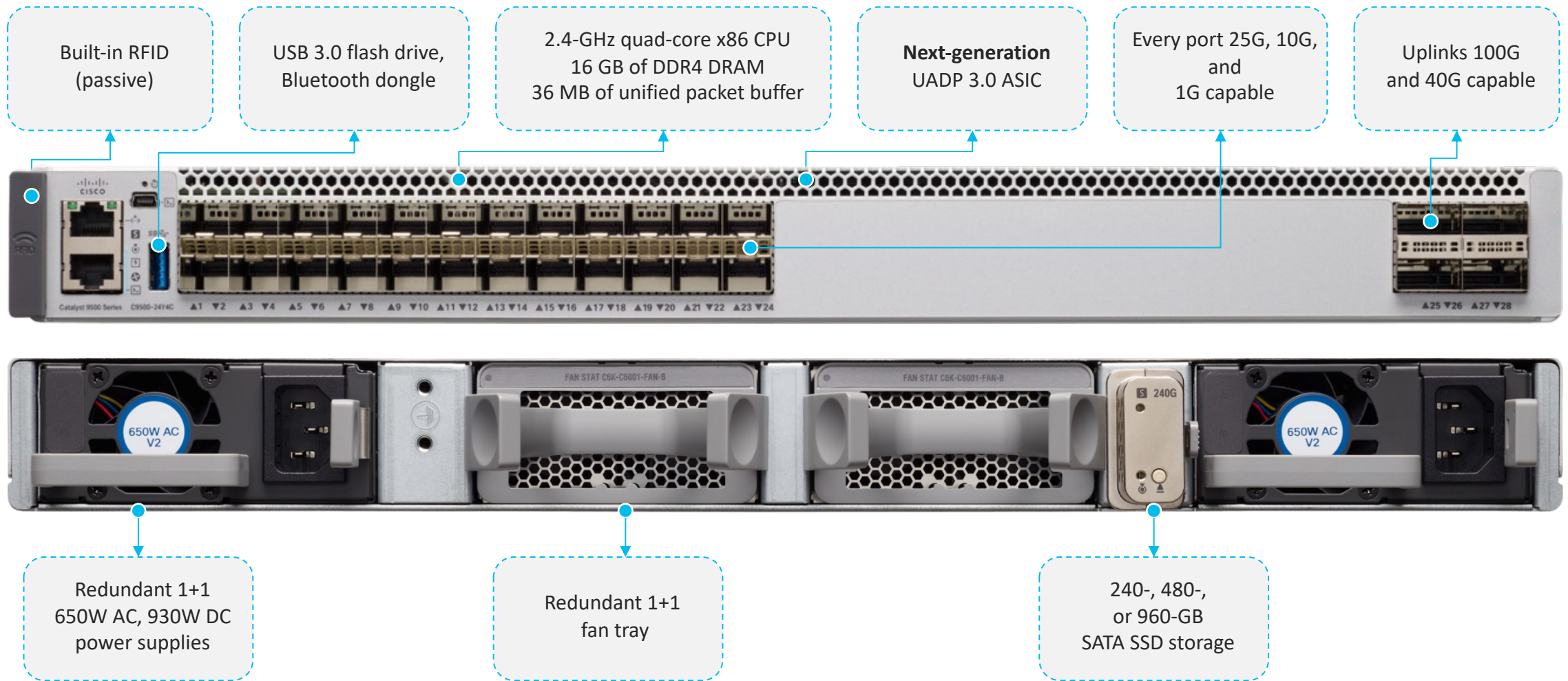
Cisco Catalyst 9500-48Y4C and 9500-24Y4C

High-level overview



Cisco Catalyst 9500-24Y4C

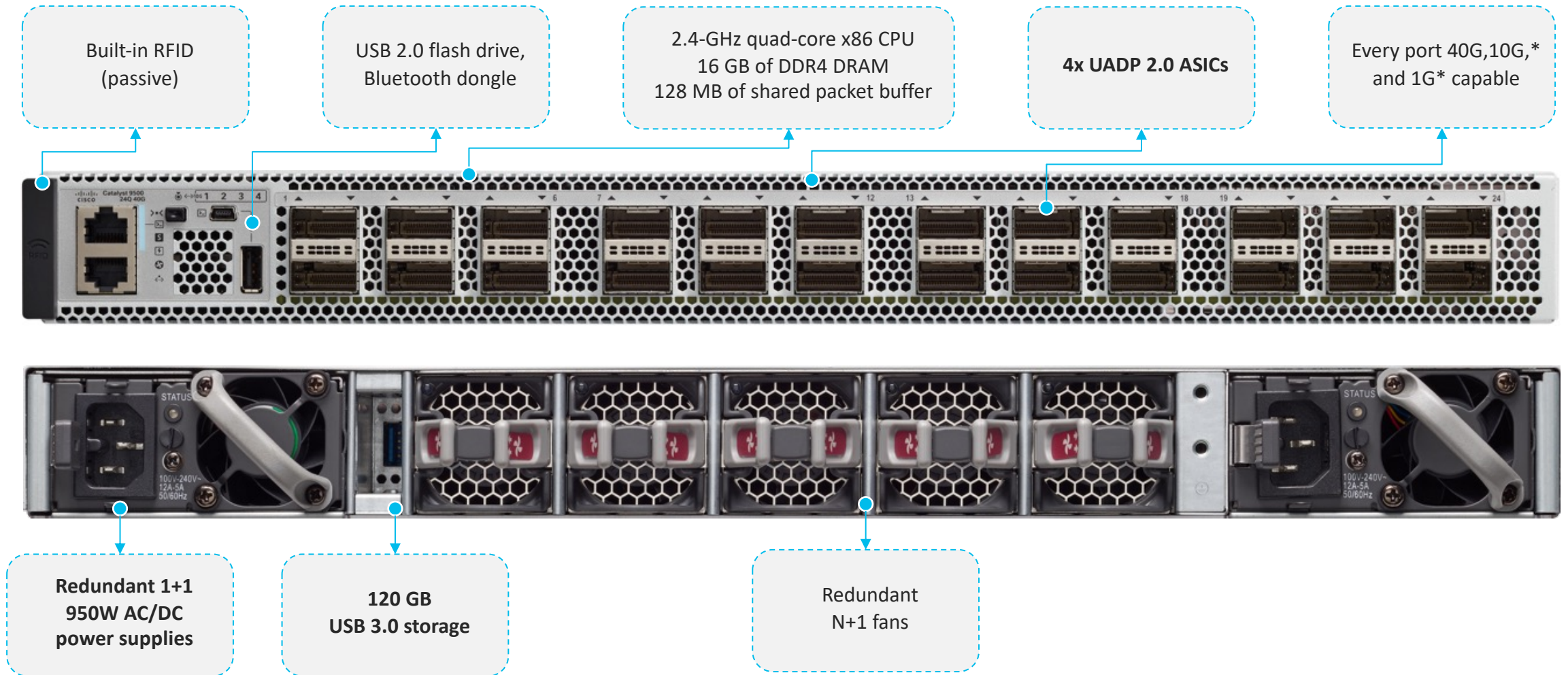
High-level overview



Cisco Catalyst 9500 Series Switches

Cisco Catalyst 9500-24Q

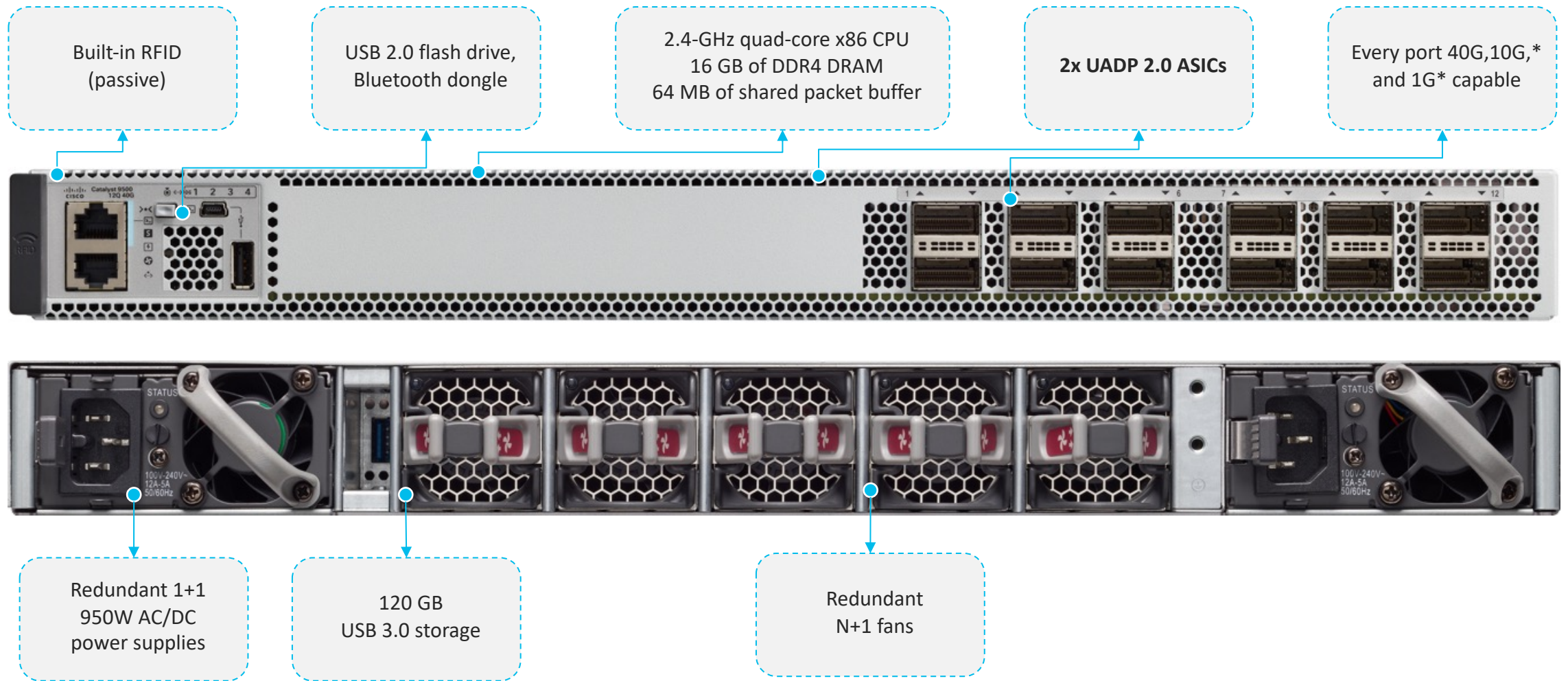
High-level overview



*With QSA adapter.

Cisco Catalyst 9500-12Q

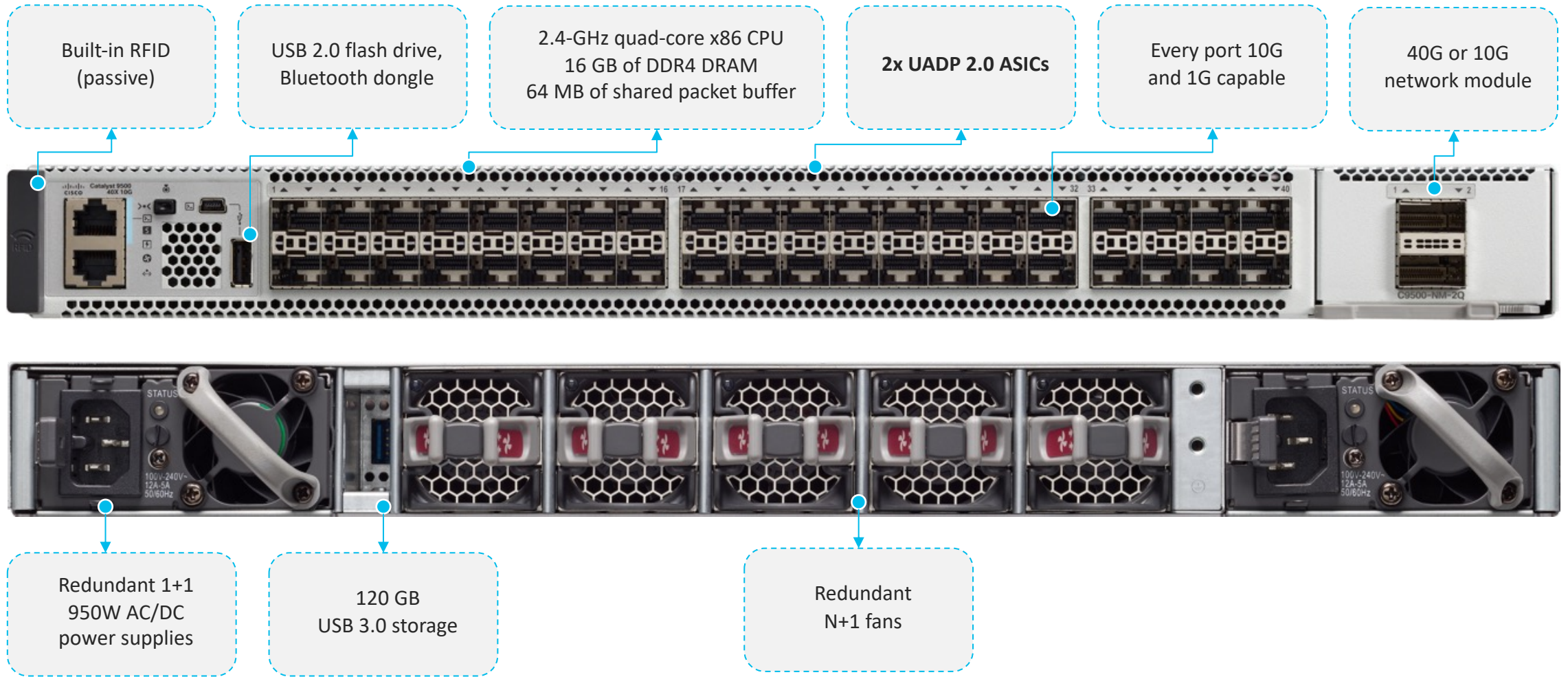
High-level overview



* With QSA adapter.

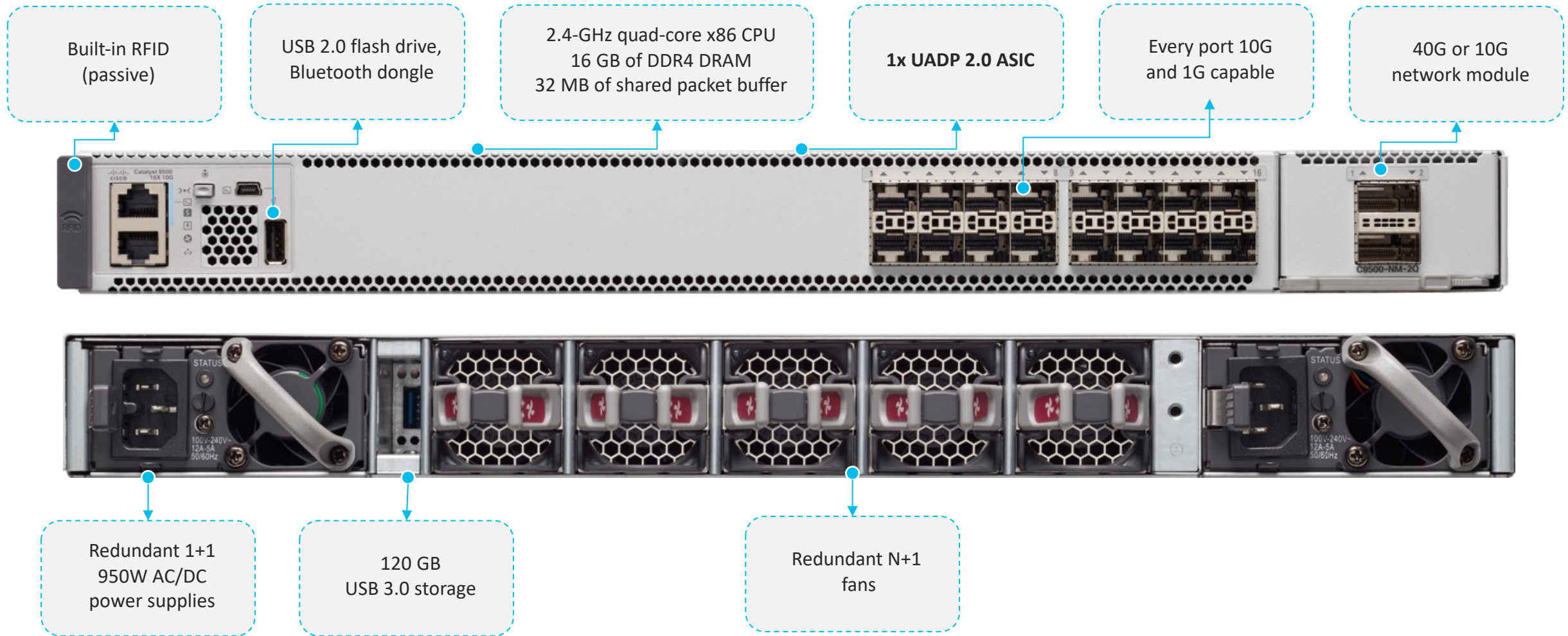
Cisco Catalyst 9500-40X

High-level overview



Cisco Catalyst 9500-16X

High-level overview



Cisco Catalyst 9500 Series

Network modules

C9500-NM-2Q

Cisco® Catalyst® 9500 Series
network module 2-port 40
Gigabit Ethernet with
QSFP+



C9500-NM-8X

Cisco Catalyst 9500 Series
network module 8-port
1/10 Gigabit Ethernet with
SFP/SFP+

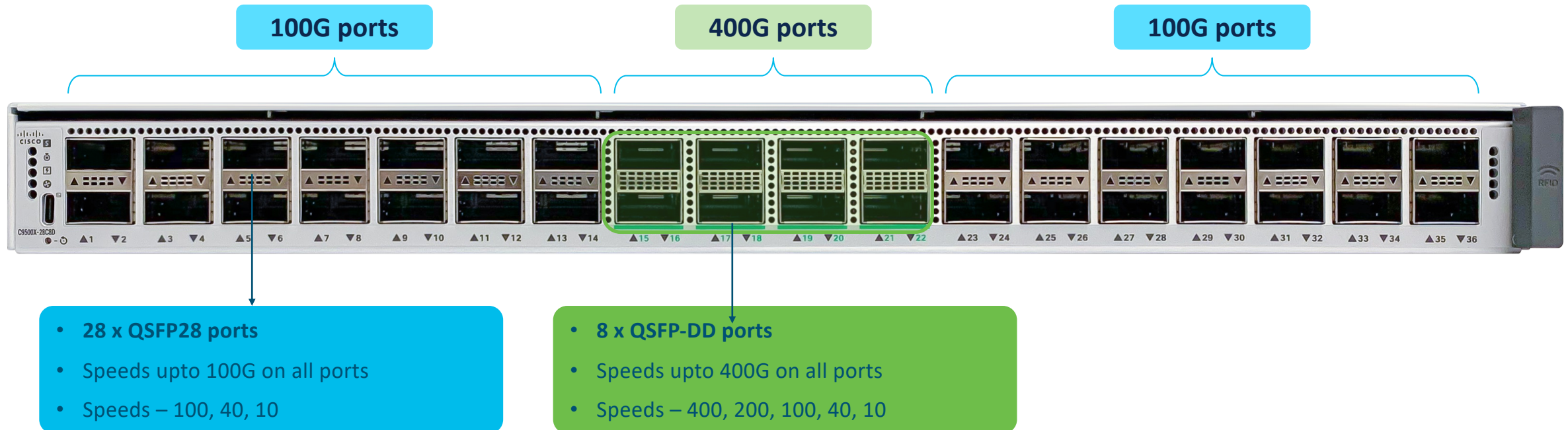


Uplink modules supported on C9500-40X and C9500-16X
Online Insertion and Removal (OIR) supported capable

Port Speeds and QSA

C9500X-28C8D

Port Speeds



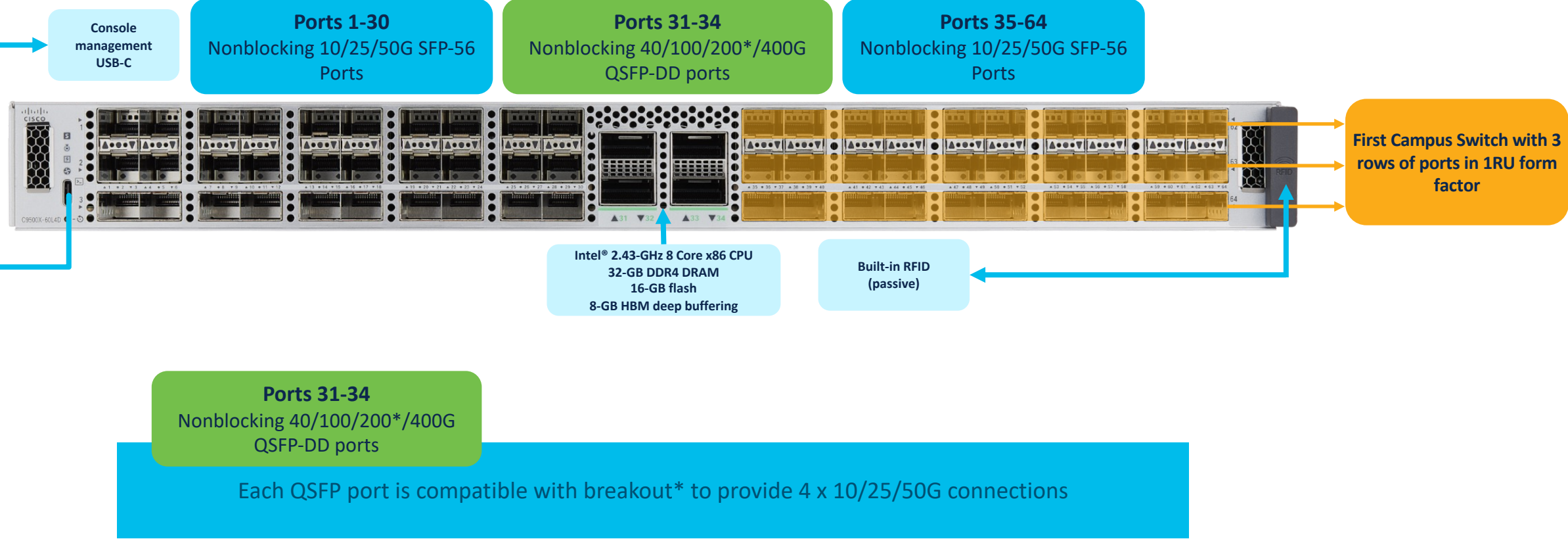
SFP breakout and QSA* support



Layer23-Switch | www.layer23-switch.com

Catalyst C9500X-60L4D

Innovative Design

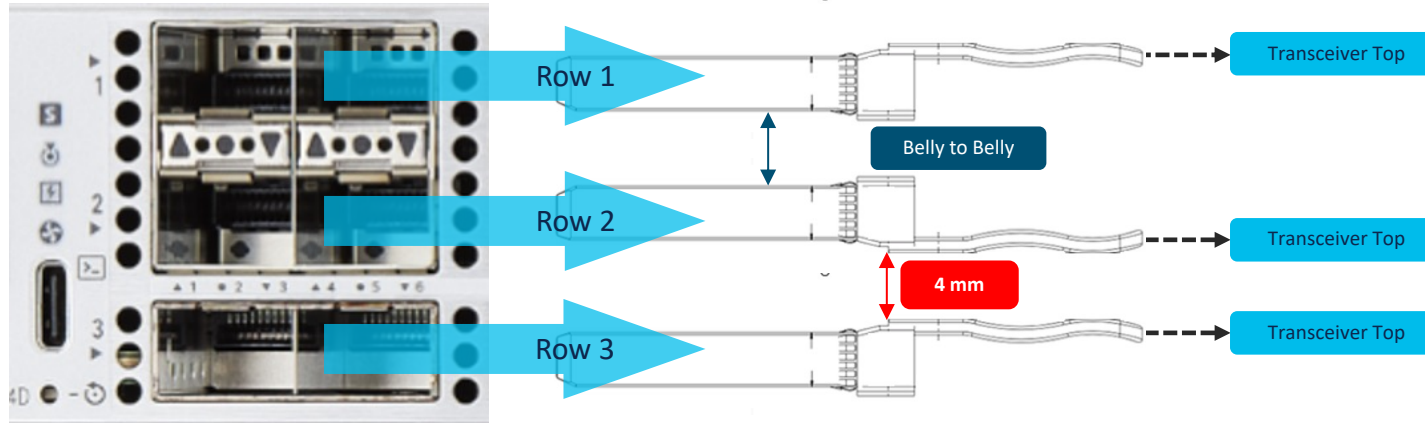


* Hardware capable. Roadmap

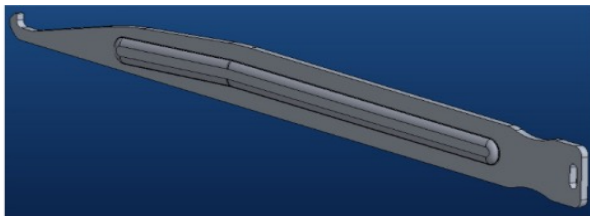
Catalyst C9500X-60L4D

Transceiver Alignment

Transceiver Alignment



- No spacing issues between Row 1 and Row 2.
- Row 1 and 2 are belly to belly with each other
- Transceiver in row 2 is inserted upside down with base of transceiver facing up
- **Minimum 4mm space between the head of transceiver in row 2 and head of transceiver in Row 3 required for smooth operation.**
- Some transceivers with bigger heads might have insufficient space when inserted both in middle and bottom rows



Low spacing between middle and bottom rows require the use of a special tool to remove transceivers without disturbing/damaging neighbouring ports.

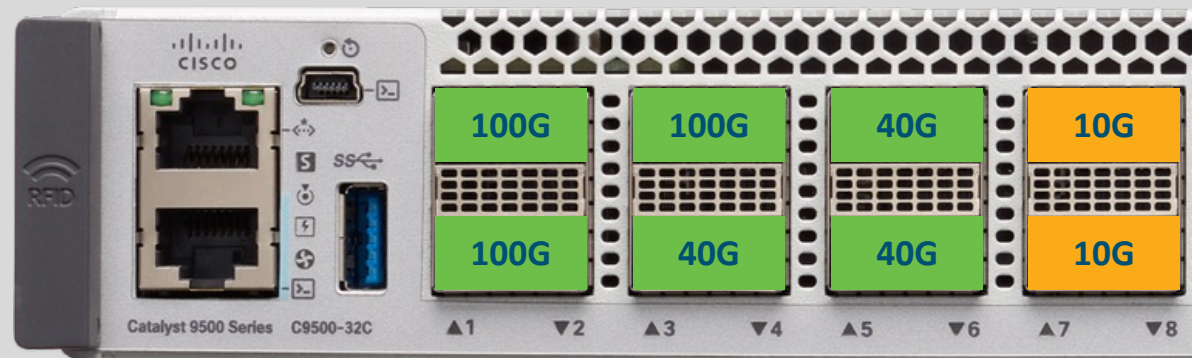
Tool included in accessory kit with each switch.

Cisco Catalyst 9500-32C

Port mode – insertion

- Ports speeds supported: 100G, 40G, 10G, 1G
- Default speed: 100G
- 100G QSFP supported on all ports
- Line rate on every port above 187-byte packet size
- Interface port speeds updated based on transceivers inserted
- Mix and match of 10G/40G and 100G speeds allowed on all ports

100G

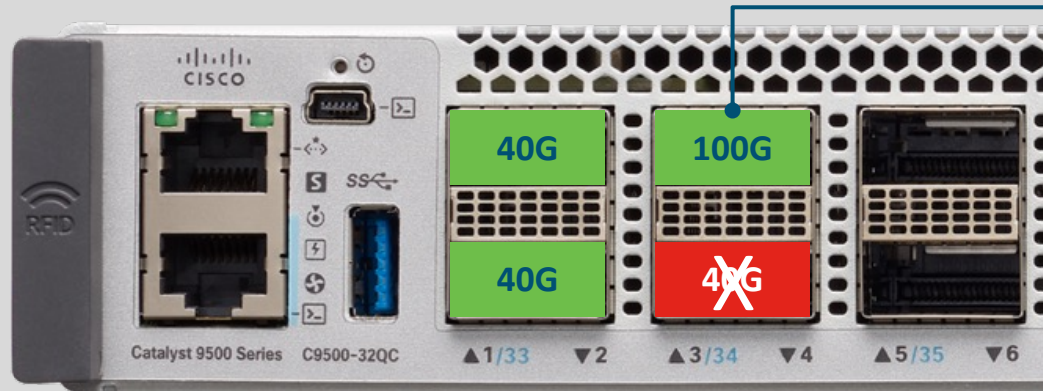


Cisco Catalyst 9500-32QC

Mode conversion – CLI based

- Port speeds supported: 10G, 40G, 100G
- Default port speed: 40G (ports 1 to 24) and 100G (ports 28 to 32)
- Line rate on every port above 187-byte packet size
- 100G QSFP supported only on upper 16 ports (ports 1 to 16)
- 100G ports are enabled using an interface CLI command disabling lower 40G ports
- Mix and match of 10G/40G and 100G ports speeds allowed

```
C9510-32QC(config)#int Hu1/0/34  
C9510-32QC(config-if)#enable  
C9510-32QC(config-if)#
```



Cisco Catalyst 9500-48Y4C

Mode conversion – insertion based

- Port speeds supported: 1G, 10G, 25G, 40G,* 100G*
- Default downlink port speed: 25G
- Default uplink port speed: 100G
- 100G QSFP supported on uplink ports only
- Line rate on every port above 187-byte packet size
- Interface port speeds updated based on transceivers inserted
- Mix and match of 1G, 10G, and 25G on downlink ports and 40G and 100G on uplink supported



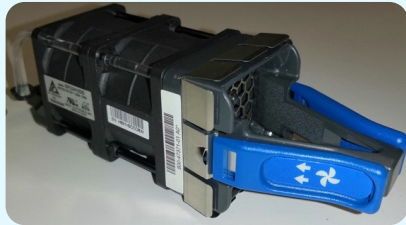
* Uplink only.

Catalyst 9500 series Power and Environment Overview

Cisco Catalyst C9500X-28C8D

Environmental overview

High-efficiency **Bi-directional**
redundant fans



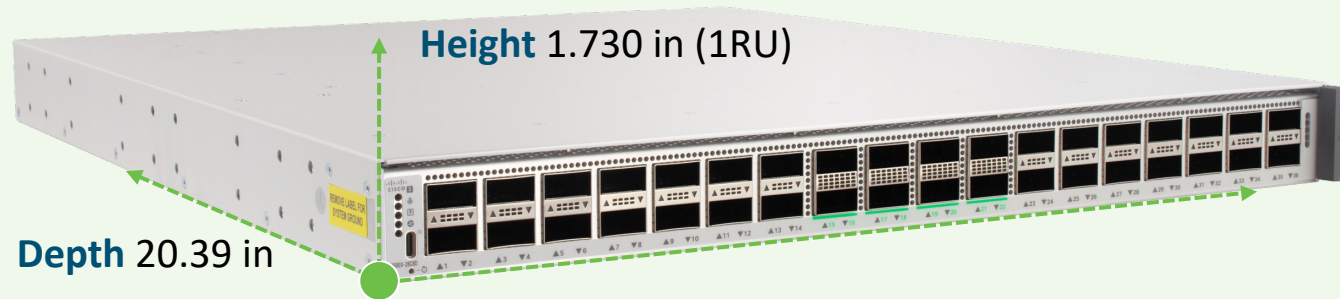
Platinum efficient **1500W**
AC/DC power supplies



AC power supply



DC power supply



Height 1.730 in (1RU)

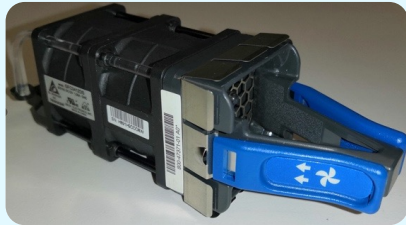
Depth 20.39 in

Width 17.50 in

Cisco Catalyst C9500X-60L4D

Environmental overview

High-efficiency **Bi-directional**
redundant fans



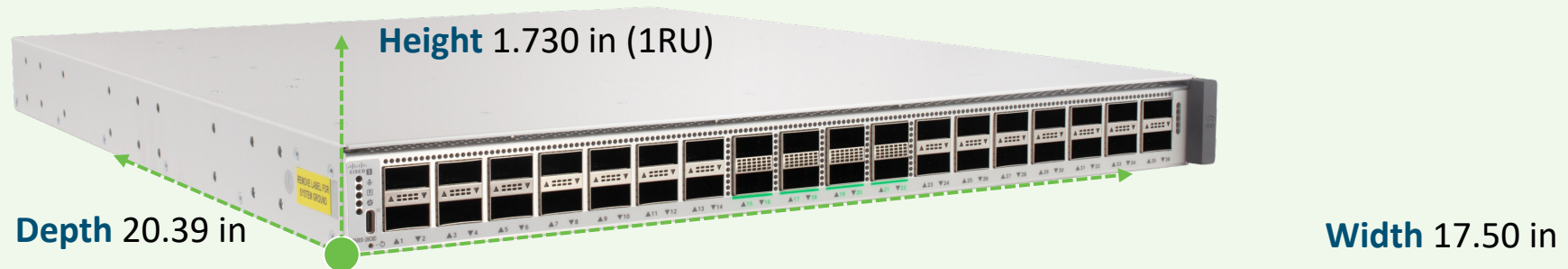
Platinum efficient **1500W**
AC/DC power supplies



AC power supply



DC power supply



Cisco Catalyst 9500-32C

Environmental overview

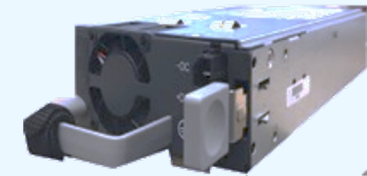
High-efficiency **24,000 rpm**
redundant fans



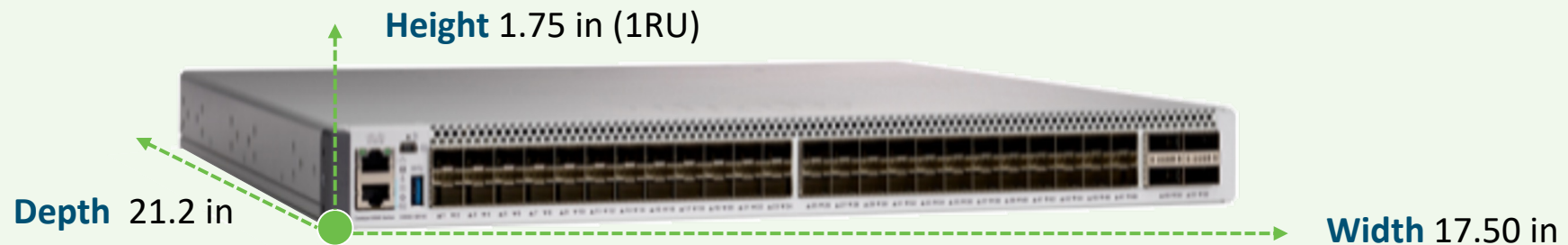
Platinum efficient **1.6kW AC/DC**
power supplies



AC PSU



DC PSU



Height 1.75 in (1RU)

Depth 21.2 in

Width 17.50 in

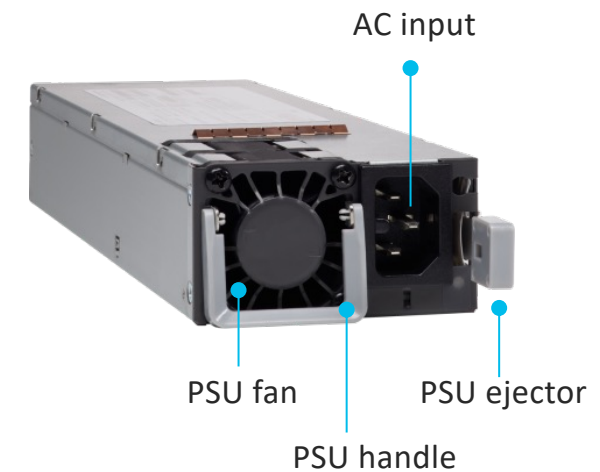
Cisco Catalyst 9500-32C

Power supply redundancy and inputs

Power supply highlights:

- Dual hot-swappable AC/DC/mixed Power Supplies (PSUs) supported
- Maximum output is 1600W at 220V and 1000W at 110V
- More than 90% power efficiency at 50% to 100% of load
- Power hold-up time is ~20 ms at 100% load
- Redundant load sharing (1+1) mode only

LED	Color	Status	Description
Green		OFF	No input
Green		Blinking	12V main off, 12V standby power ON
Green		Solid	12V main ON
Yellow		OFF	No warnings or errors
Yellow		Blinking	Warning detected, 12V main
Yellow		Solid	Critical error detected



Cisco Catalyst 9500-32C

Fan redundancy and airflow

Highlights:

- 5 variable-speed high-efficiency fans at rear of chassis
- Thermal sensor to detect ambient temperature and adjust fan speeds
- Fans are hot-swappable
- Front-to-back airflow
- Can still operate with one fan unit failure

LED	Color	Status	Description
Fan		Solid	All fans OK
Fan		Solid	One fan faulty
Fan		Solid	One or more fans faulty Exceeded limit



Cisco Catalyst 9500-32QC, -48Y4C, and -24Y4C

Environmental overview

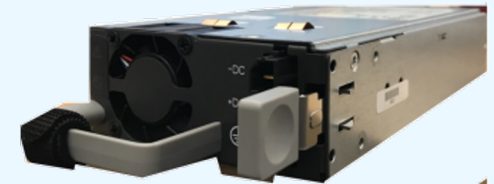
High-efficiency **20,000 rpm**
redundant fans



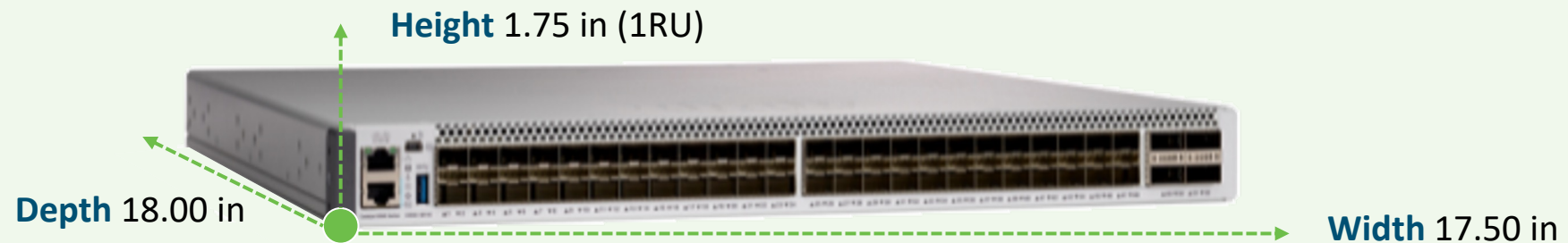
Platinum efficient **650W or 930W**
power supply



AC power supply



DC power supply



Height 1.75 in (1RU)

Depth 18.00 in

Width 17.50 in

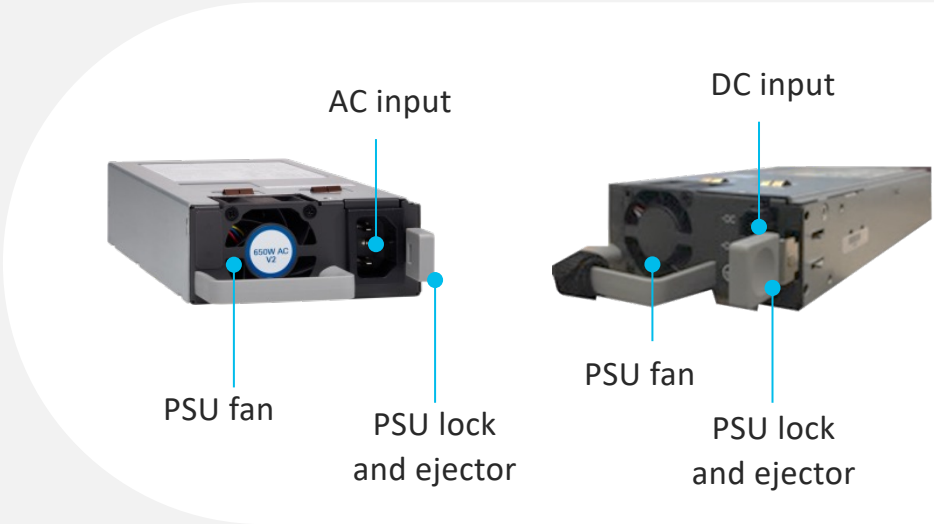
Cisco Catalyst 9500-32QC, -48Y4C, and -24Y4C

Power supply redundancy and inputs

Power supply highlights:

- Dual hot-swappable AC/DC/mixed power supplies supported
- Maximum output 12V/650W at 220V/110V AC Input
- More than 90% power efficiency at 50% to 100% of load
- Power hold-up time is <20 ms at 90% load
- Redundant load sharing (1+1) mode only

LED	Color	Status	Description
Green		OFF	No input
Green		Blinking	12V main off, 12V standby power ON
Green		Solid	12V main ON
Yellow		OFF	No warnings or errors
Yellow		Blinking	Warning detected, 12V main
Yellow		Solid	Critical error detected



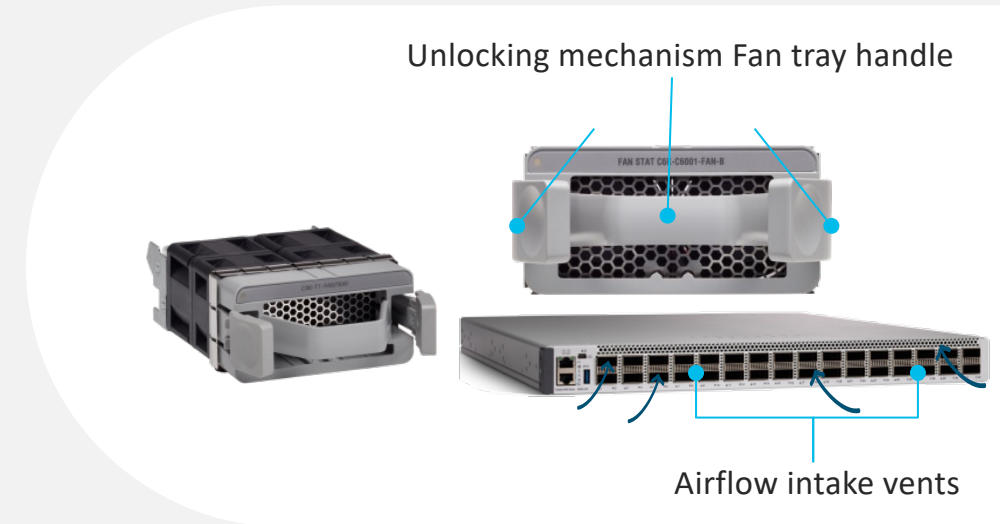
Cisco Catalyst 9500-32QC, -48Y4C, and -24Y4C

Fan redundancy and airflow

Highlights

- Dual variable-speed high-efficiency fan trays
- Thermal sensor to detect ambient temperature and adjust fan speeds
- Fan trays are hot-swappable
- Front-to-back airflow
- Can still operate with individual fan tray failure

LED	Color	Status	Description
FAN		Solid	Fan tray OK
FAN		Solid	Fan tray fault



Cisco Catalyst 9500 Series

Environmental overview

High-efficiency **24,000 rpm**
redundant fans



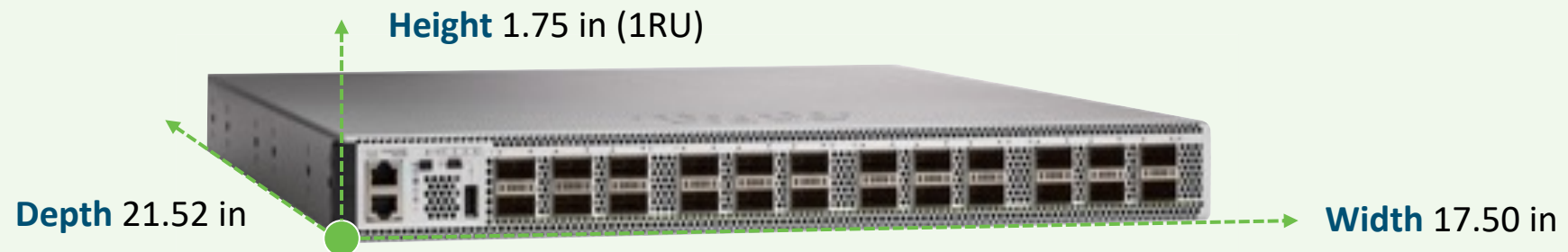
Platinum efficient **950W**
AC/DC power supplies



AC power supply



DC power supply



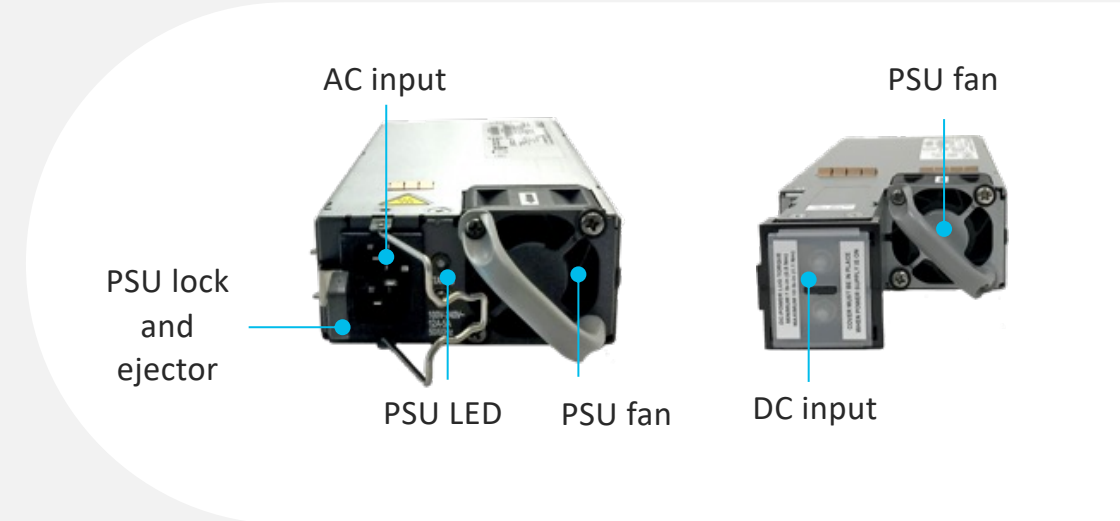
Cisco Catalyst 9500-24Q, -12Q, -40x, and -16x

Power supply redundancy and inputs

Power supply highlights:

- Dual hot-swappable AC/DC/mixed power supplies supported
- Maximum output 12V/950W at 220V/110V AC input
- More than 90% power efficiency at 50% to 100% of load
- Redundant load sharing (1+1) mode only
- **1 power supply** sufficient to power up switch
- Single bicolor LED to indicate PSU status
- Variable-speed fan with inside-to-outside and front-to-back airflow

LED	Color	Status	Description
Green		Solid	PSU operating normally, 12V main ON
Amber		Solid	PSU input loss
Red		Solid	PSU output failure



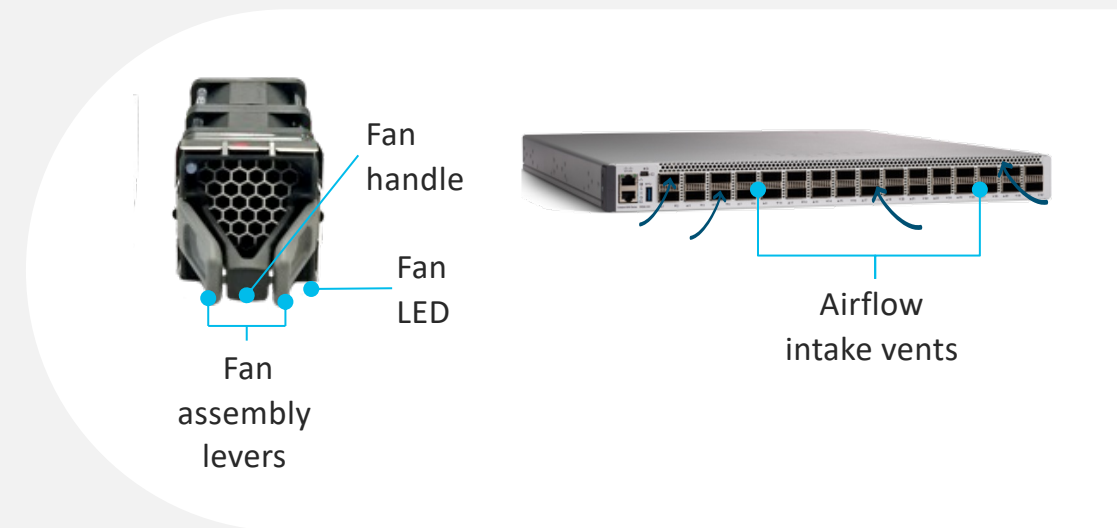
Cisco Catalyst 9500-24Q, -12Q, -40x, and 16x

Fan redundancy and airflow

Power supply highlights:

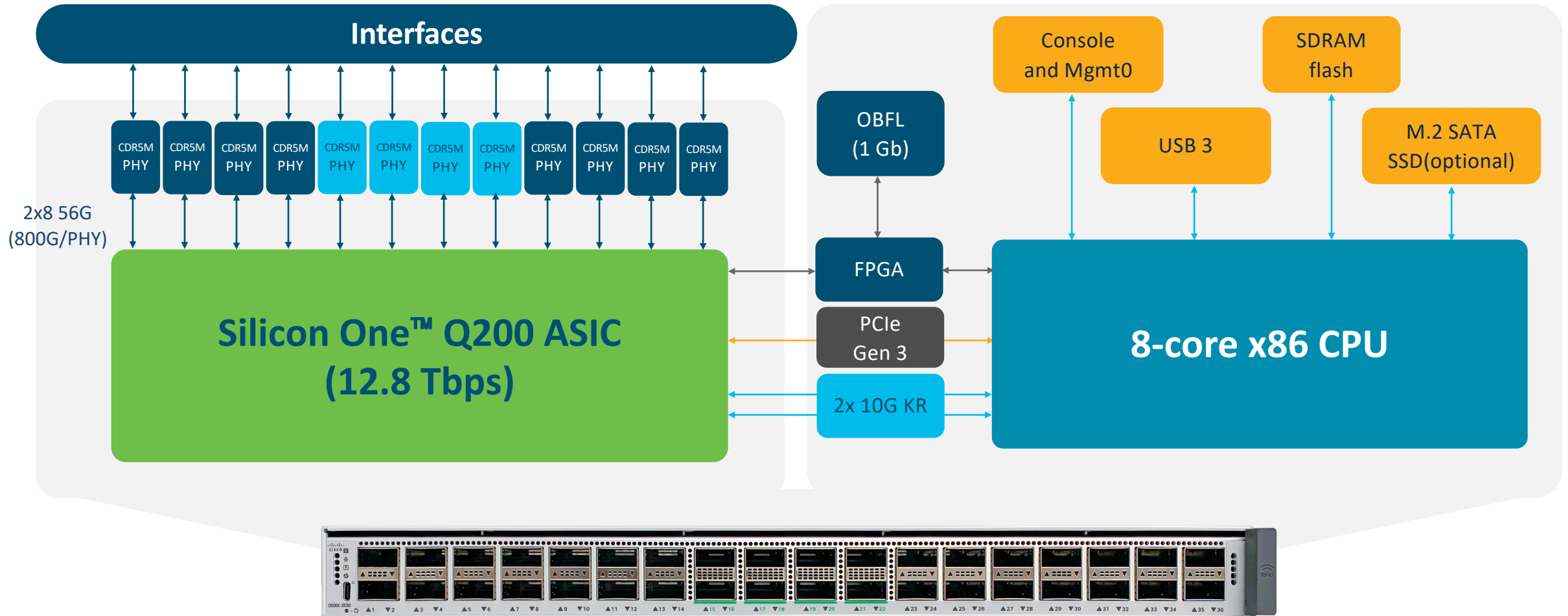
- N+1 variable-speed high-efficiency fans
- Thermal sensor to detect ambient temperature and adjust fan speeds
- Individual fans are OIR capable up to 120 seconds
- Front-to-back airflow
- Can still operate with individual fan tray failure

Color	Status	Description
	Off	The fan tray is not receiving power; the fans have stopped
	Solid	All fans are operating normally
	Solid	One or more fans have encountered tachometer faults
	Solid	One or more fans' tachometer faults have exceeded the maximum limit



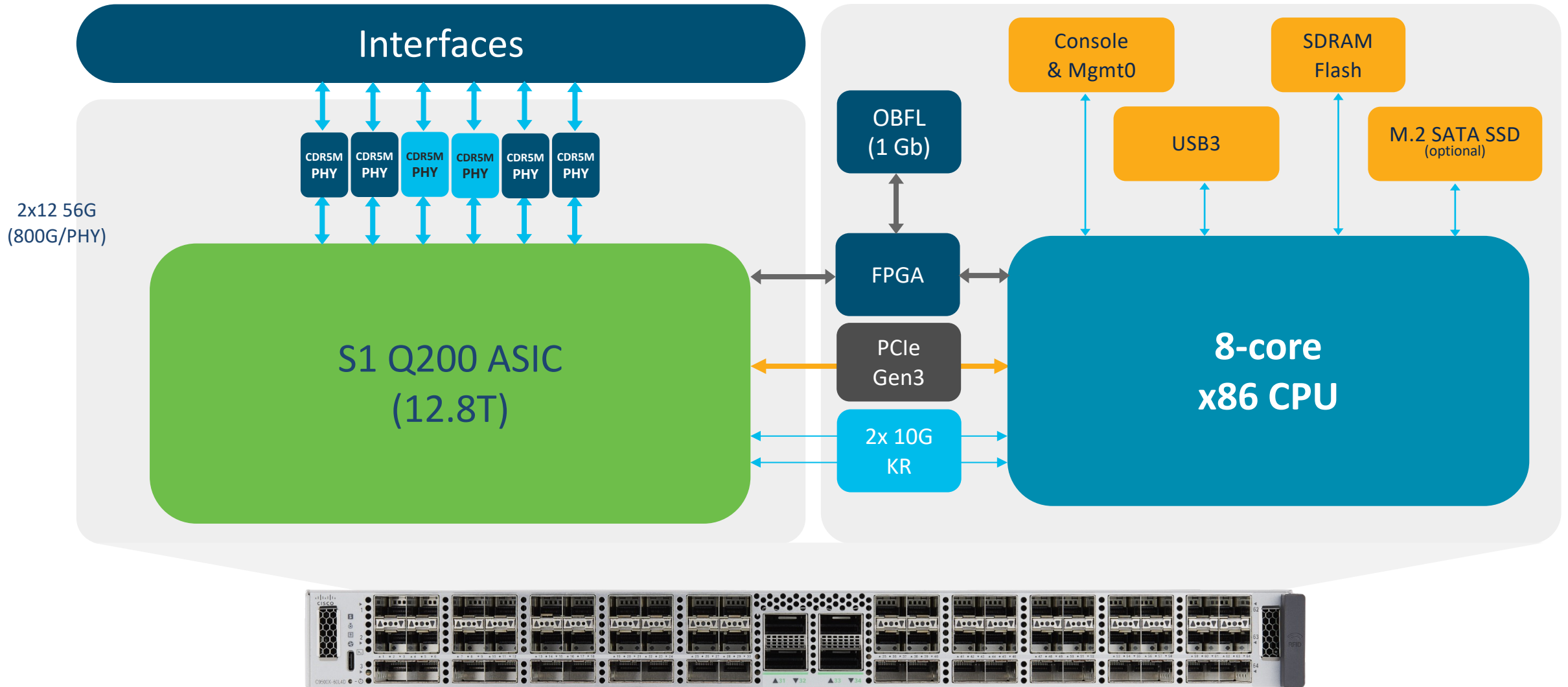
Architecture

C9500X-28C8D block diagram



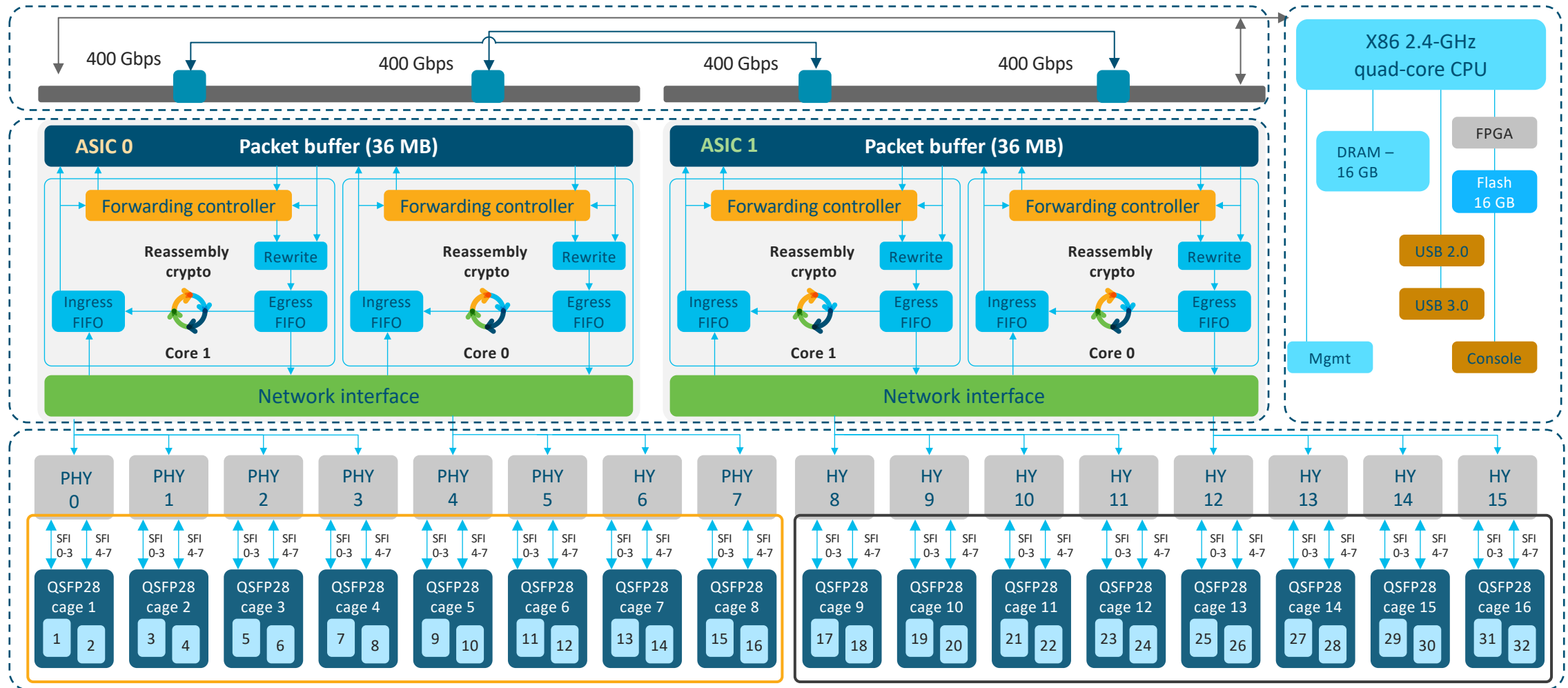
C9500X-60L4D Block Diagram

Gen2 Fixed 1RU QSFP Switch - 60x50G and 4x100/400G



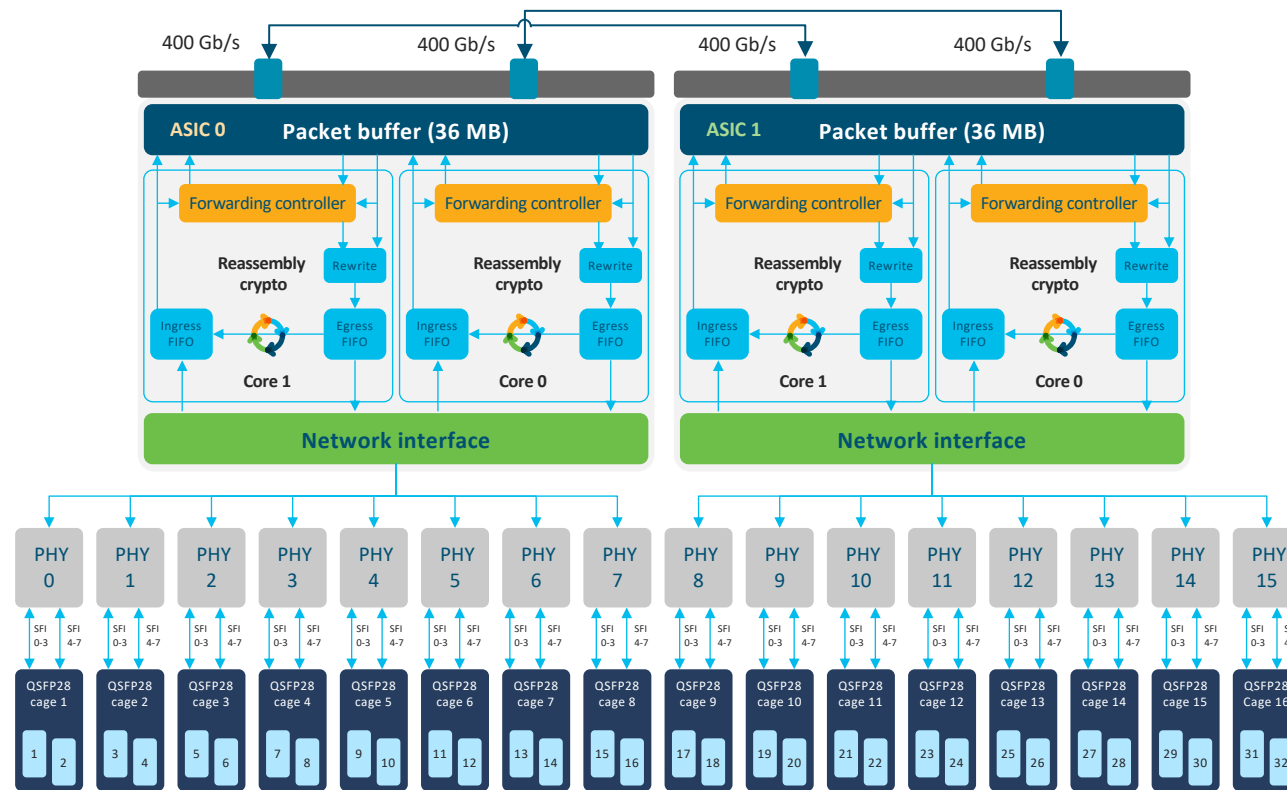
Cisco Catalyst 9500-32C

Block diagram



Cisco Catalyst 9500-32C

Port-to-ASIC mapping



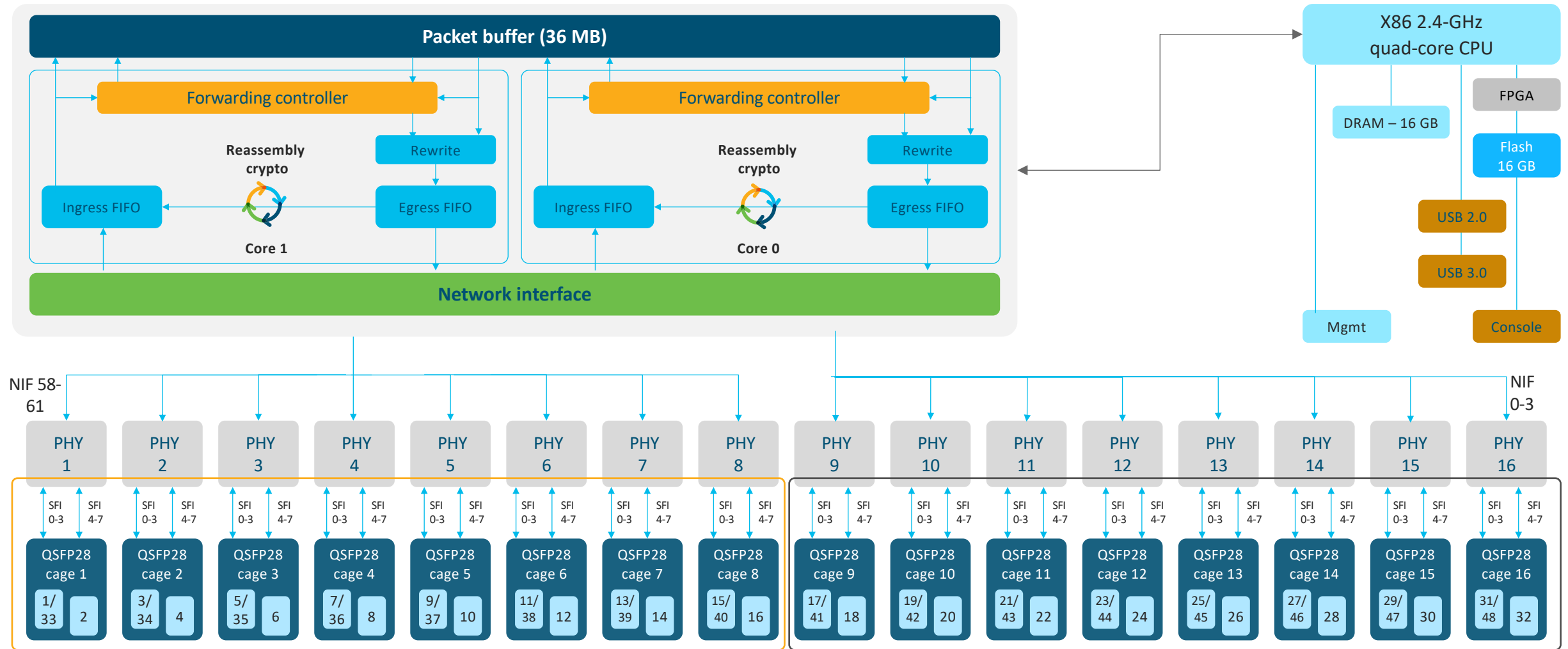
Command to verify the port-to-ASIC mapping:
show platform software fed active ifm mappings

```
C9500H-32C#show platform software fed active ifm mapping
```

Interface	IF_ID	Inst	Asic	Core	Port	SubPort	Mac	Cntx	LPN	GPN	Type	Active
HundredGigE1/0/1	0x6	1	0	1	16	0	16	2	1	101	NIF	Y
HundredGigE1/0/2	0x7	1	0	1	17	0	20	6	2	102	NIF	Y
HundredGigE1/0/3	0x8	1	0	1	18	0	24	10	3	103	NIF	Y
HundredGigE1/0/4	0x9	1	0	1	19	0	28	14	4	104	NIF	Y
HundredGigE1/0/5	0xa	1	0	1	0	0	0	2	5	105	NIF	Y
HundredGigE1/0/6	0xb	1	0	1	1	0	4	6	6	106	NIF	Y
HundredGigE1/0/7	0xc	1	0	1	2	0	8	10	7	107	NIF	Y
HundredGigE1/0/8	0xd	1	0	1	3	0	12	14	8	108	NIF	Y
HundredGigE1/0/9	0xe	0	0	0	16	0	28	2	9	109	NIF	Y
HundredGigE1/0/10	0xf	0	0	0	17	0	24	6	10	110	NIF	Y
HundredGigE1/0/11	0x10	0	0	0	18	0	20	10	11	111	NIF	Y
HundredGigE1/0/12	0x11	0	0	0	19	0	16	14	12	112	NIF	Y
HundredGigE1/0/13	0x12	0	0	0	0	0	12	2	13	113	NIF	Y
HundredGigE1/0/14	0x13	0	0	0	1	0	8	6	14	114	NIF	Y
HundredGigE1/0/15	0x14	0	0	0	2	0	4	10	15	115	NIF	Y
HundredGigE1/0/16	0x15	0	0	0	3	0	0	14	16	116	NIF	Y
HundredGigE1/0/17	0x16	3	1	1	16	0	16	2	17	117	NIF	Y
HundredGigE1/0/18	0x17	3	1	1	17	0	20	6	18	118	NIF	Y
HundredGigE1/0/19	0x18	3	1	1	18	0	24	10	19	119	NIF	Y
HundredGigE1/0/20	0x19	3	1	1	19	0	28	14	20	120	NIF	Y
HundredGigE1/0/21	0x1a	3	1	1	0	0	0	2	21	121	NIF	Y
HundredGigE1/0/22	0x1b	3	1	1	1	0	4	6	22	122	NIF	Y
HundredGigE1/0/23	0x1c	3	1	1	2	0	8	10	23	123	NIF	Y
HundredGigE1/0/24	0x1d	3	1	1	3	0	12	14	24	124	NIF	Y
HundredGigE1/0/25	0x1e	2	1	0	16	0	28	2	25	125	NIF	Y
HundredGigE1/0/26	0x1f	2	1	0	17	0	24	6	26	126	NIF	Y
HundredGigE1/0/27	0x20	2	1	0	18	0	20	10	27	127	NIF	Y
HundredGigE1/0/28	0x21	2	1	0	19	0	16	14	28	128	NIF	Y
HundredGigE1/0/29	0x22	2	1	0	0	0	12	2	29	129	NIF	Y
HundredGigE1/0/30	0x23	2	1	0	1	0	8	6	30	130	NIF	Y
HundredGigE1/0/31	0x24	2	1	0	2	0	4	10	31	131	NIF	Y
HundredGigE1/0/32	0x25	2	1	0	3	0	0	14	32	132	NIF	Y

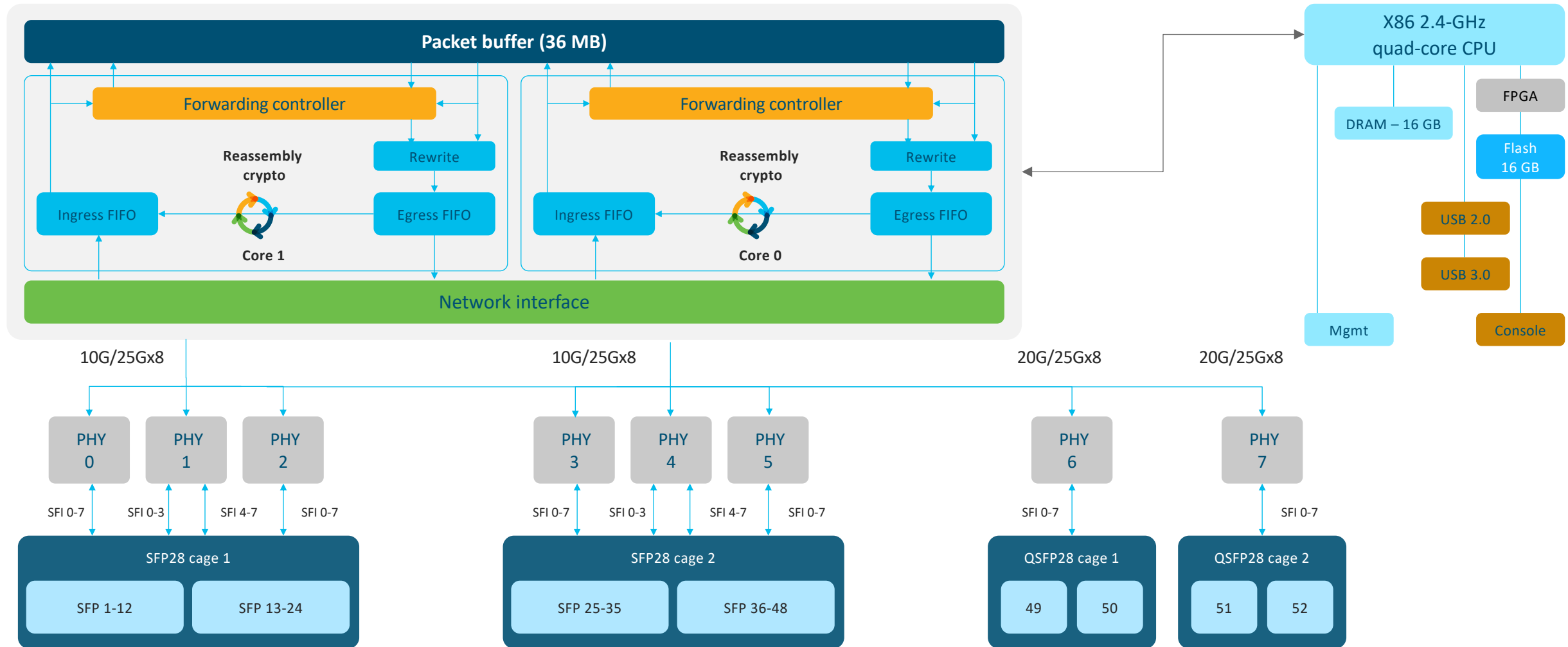
Cisco Catalyst 9500-32QC

Block diagram



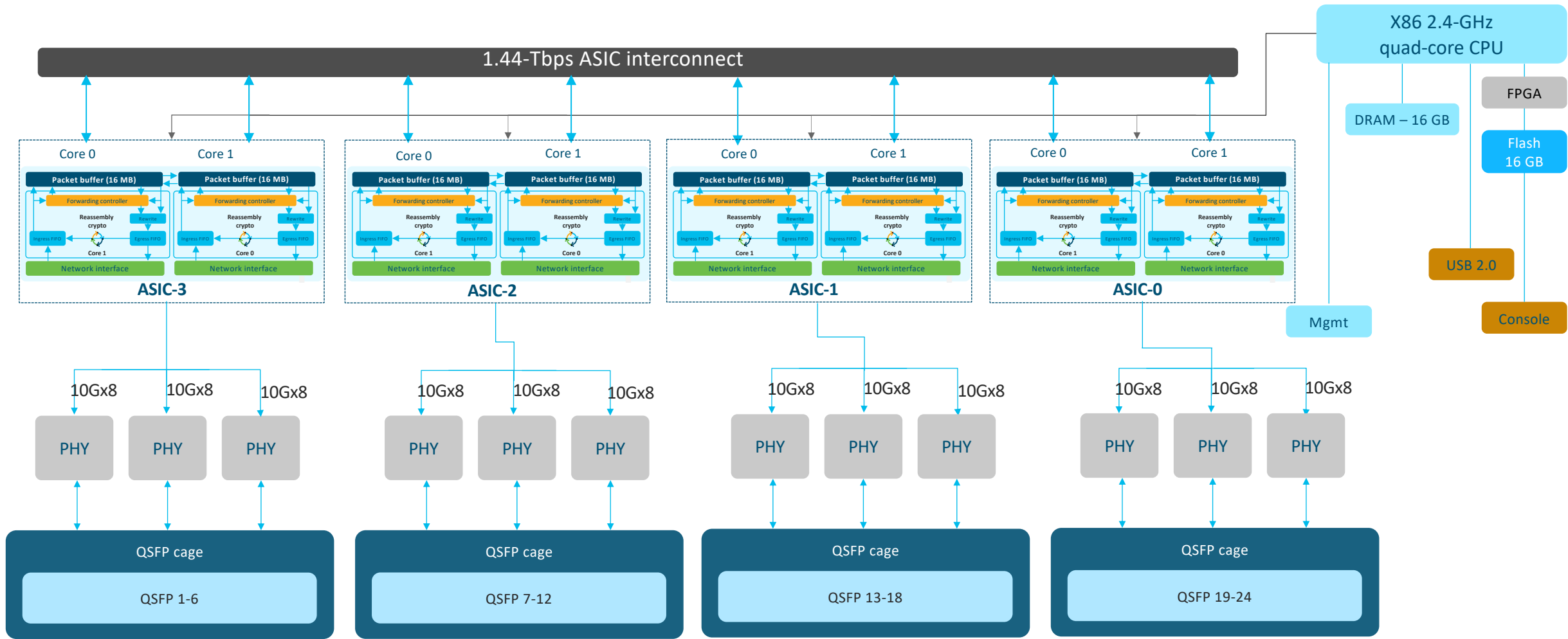
Cisco Catalyst 9500-48Y4C

Block diagram



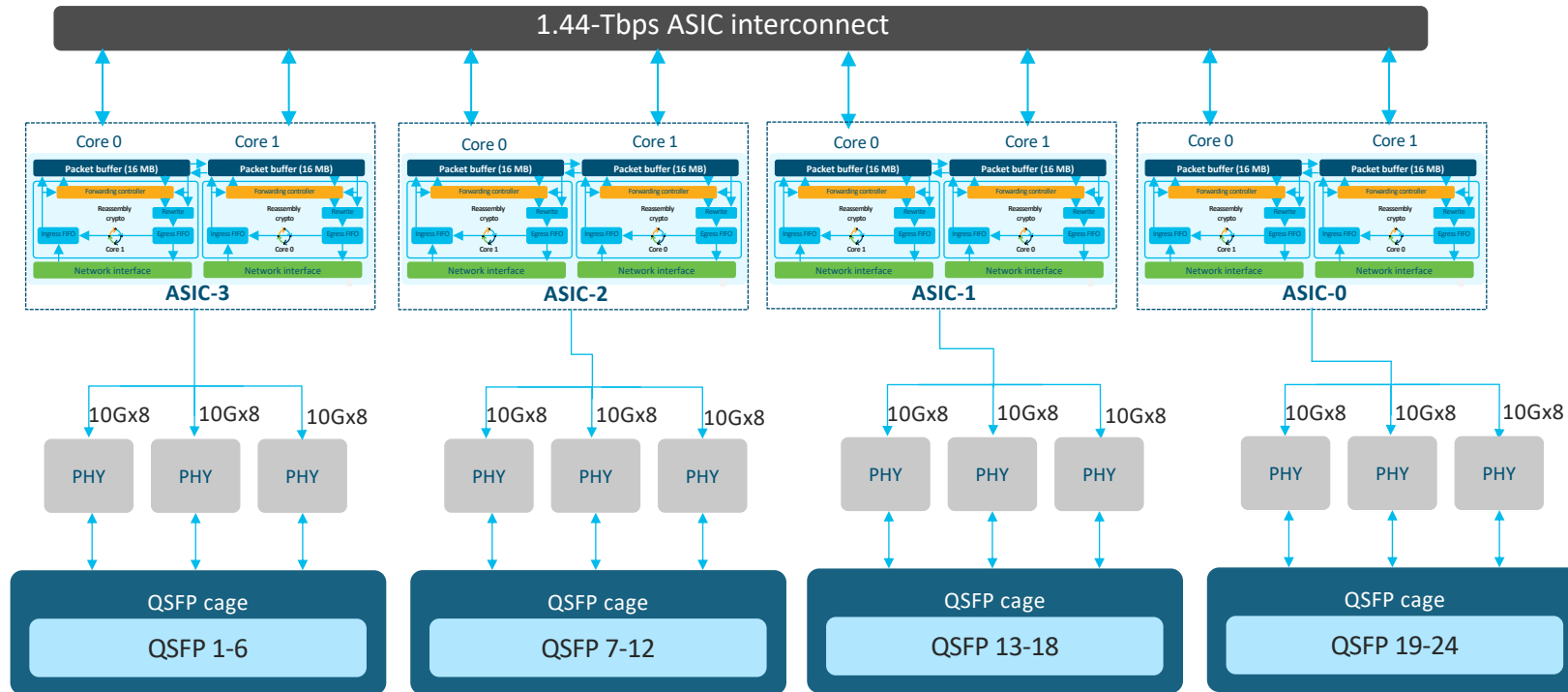
Cisco Catalyst 9500-24Q

Block diagram



Cisco Catalyst 9500-24Q

Port-to-ASIC mapping



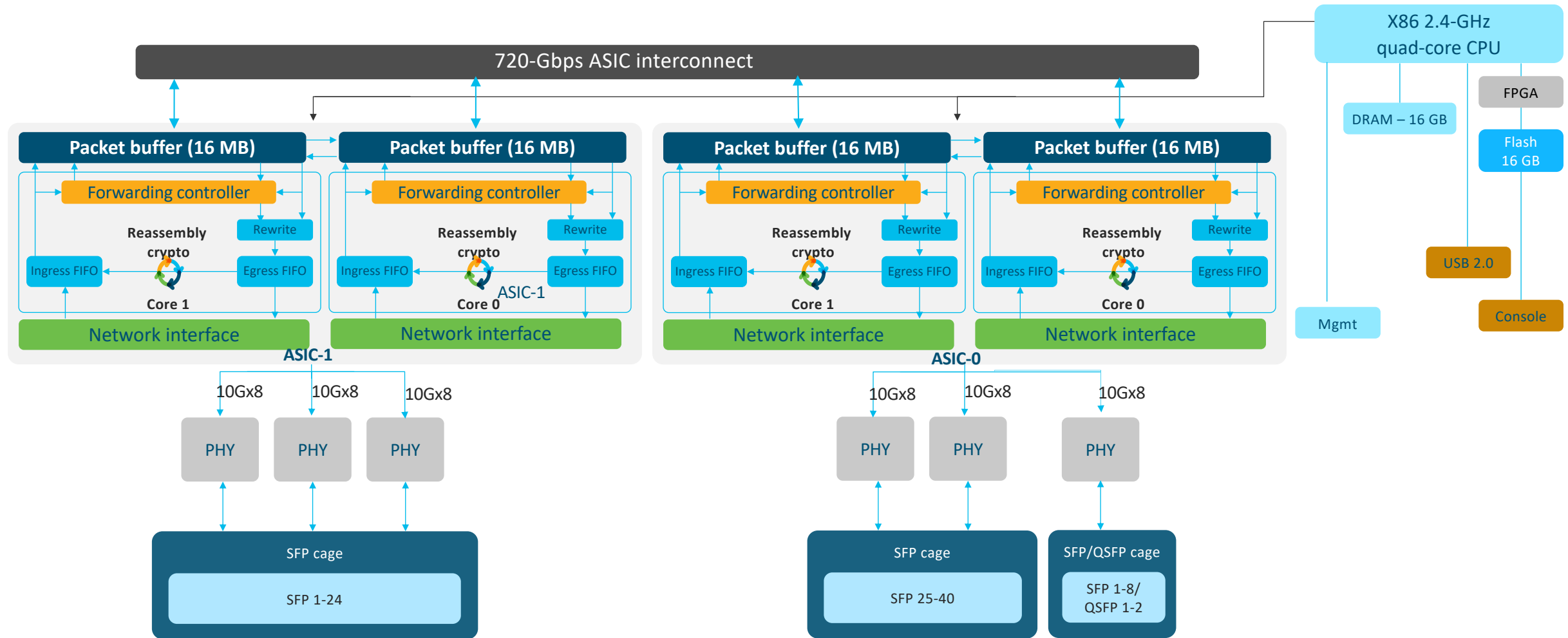
```
C9500-24Q#sh platform software fed switch active ifm mappings lpn
Mappings Table
```

LPN	ASIC	Port	Interface	IF_ID	Active
1	3	0	FortyGigabitEthernet1/0/1	0x00000007	Y
2	3	1	FortyGigabitEthernet1/0/2	0x00000008	Y
3	3	2	FortyGigabitEthernet1/0/3	0x00000009	Y
4	3	3	FortyGigabitEthernet1/0/4	0x0000000a	Y
5	3	4	FortyGigabitEthernet1/0/5	0x0000000b	Y
6	3	5	FortyGigabitEthernet1/0/6	0x0000000c	Y
7	2	6	FortyGigabitEthernet1/0/7	0x0000000d	Y
8	2	7	FortyGigabitEthernet1/0/8	0x0000000e	Y
9	2	8	FortyGigabitEthernet1/0/9	0x0000000f	Y
10	2	9	FortyGigabitEthernet1/0/10	0x00000010	Y
11	2	10	FortyGigabitEthernet1/0/11	0x00000011	Y
12	2	11	FortyGigabitEthernet1/0/12	0x00000012	Y
13	1	12	FortyGigabitEthernet1/0/13	0x00000013	Y
14	1	13	FortyGigabitEthernet1/0/14	0x00000014	Y
15	1	14	FortyGigabitEthernet1/0/15	0x00000015	Y
16	1	15	FortyGigabitEthernet1/0/16	0x00000016	Y
17	1	16	FortyGigabitEthernet1/0/17	0x00000017	Y
18	1	17	FortyGigabitEthernet1/0/18	0x00000018	Y
19	0	18	FortyGigabitEthernet1/0/19	0x00000019	Y
20	0	19	FortyGigabitEthernet1/0/20	0x0000001a	Y
21	0	20	FortyGigabitEthernet1/0/21	0x0000001b	Y
22	0	21	FortyGigabitEthernet1/0/22	0x0000001c	Y
23	0	22	FortyGigabitEthernet1/0/23	0x0000001d	Y
24	0	23	FortyGigabitEthernet1/0/24	0x0000001e	Y

Command to verify the port-to-ASIC mapping:
 show platform software fed switch active ifm mappings lpn

Cisco Catalyst 9500-40X

Block diagram



Cisco Catalyst 9500 Series

User-centric platform design

Cisco Catalyst 9500 Series

Blue beacon

- Blue beacon LED allows easy identification of the switch being accessed
- Color/state: Solid blue
- Blue beacon can be turned on using Exec mode Command-Line Interface (CLI)

Cisco® Catalyst® 9500 Series High Performance

C9500-32QC#**hw-module beacon RP active?**

Off Turn off

on Turn on

status Slot Beacon Status

C9500-32QC#**hw-module beacon RP active on**

*Jan 23 22:39:05.972: %PLATFORM_LED-6-BEACON_LED_TURNED: Slot 1 Beacon LED turned ON

C9500-32QC#**hw-module beacon RP active status**

BLUE

C9500-32QC#**hw-module beacon RP active off**

*Jan 23 22:40:39.660: %PLATFORM_LED-6-BEACON_LED_TURNED: Slot 1 Beacon LED turned OFF

C9500-32QC#**hw-module beacon RP active status**

BLACK



C9500-32C#hw-module beacon ssd on

Cisco Catalyst 9500 Series



C9500-24Q(config)#**hw-module beacon on switch 1**

*Apr 4 23:59:36.610: %PLATFORM_LED-6-BEACON_LED_TURNED: Switch 1 Beacon LED turned ON

C9500-24Q #**show hardware led | in BEACON**

BEACON: BLUE

C9500-24Q(config)#**hw-module beacon off switch 1**

*Apr 5 00:03:33.336: %PLATFORM_LED-6-BEACON_LED_TURNED: Switch 1 Beacon LED turned OFF

C9500-24Q #**show hardware led | in BEACON**

BEACON: BLACK

Cisco Catalyst 9500 Series

LEDs



System LED	Off	System is not powered on
	Green	System is operating normally
	Blinking green	System is in Rommon mode
	Amber	System temperature is exceeding max or min threshold
	Blinking amber	Faulty hardware
Beacon LED	Solid blue	The operator has indicated that the system needs attention
PSU LED	Green	Both PSUs in bay with active power
	Amber	Missing PSU or no power feed
Fan LED	Green	Fans operating normally
	Red	Fan or fans faulty

Cisco Catalyst 9500X Switch

SSD storage



M2 SATA
SSD

Use cases

- General-purpose storage
- App hosting
- Wireshark on board
- Logging local NetFlow record storage

Capabilities	
Form factor	M2 SATA
Capacity	240 GB, 480 GB, or 960 GB
Performance	300 MBps read, 290 MBps write
Power write	4.5W
Security	Hardware-based AES 256-bit

Product ID	Release
C9K-F3-SSD-240G	17.7.1
C9K-F3-SSD-480G	
C9K-F3-SSD-960G	

Cisco Catalyst 9500 Series High Performance

SSD storage



M2 SATA
SSD



Use cases

- General-purpose storage
- App hosting
- Wireshark on board
- Logging local NetFlow record storage

Capabilities

Form factor	M2 SATA
Capacity	240 GB, 480 GB, or 960 GB
Performance	300 MBps read, 290 MBps write
Power write	4.5W
Security	Hardware-based AES 256-bit

Product ID

Release

C9K-F1-SSD-240G	16.8.1a
C9K-F1-SSD-480G	
C9K-F1-SSD-960G	

Cisco Catalyst 9500 Series

USB 3.0 storage



USB 3.0
120-GB SSD



Use cases

- General-purpose storage
- App hosting
- Wireshark on board
- Logging local NetFlow record storage

Capabilities

Form factor	USB 3.0
Capacity	120 GB
Performance	400 MBps read, 140 MBps write
Power write	4.5W maximum
Security	Hardware-based AES 256-bit

Product ID	Release
SSD-120G/SSD-120G=	16.8.1a

Cisco Catalyst 9500 Series

Power supply redundancy

Redundant mode (default)



PSU1



PSU2

- Load sharing and redundancy are enabled automatically
- Each power supply provides about 50% of capacity
- This is the recommended and only mode

Redundant mode (failure)



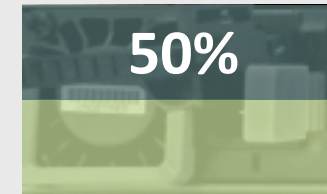
PSU1



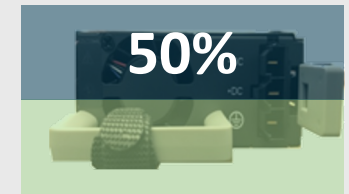
PSU2

- In case of power supply or power feed failure, the active power supply operates at 100% capacity

AC/DC power supplies



PSU1



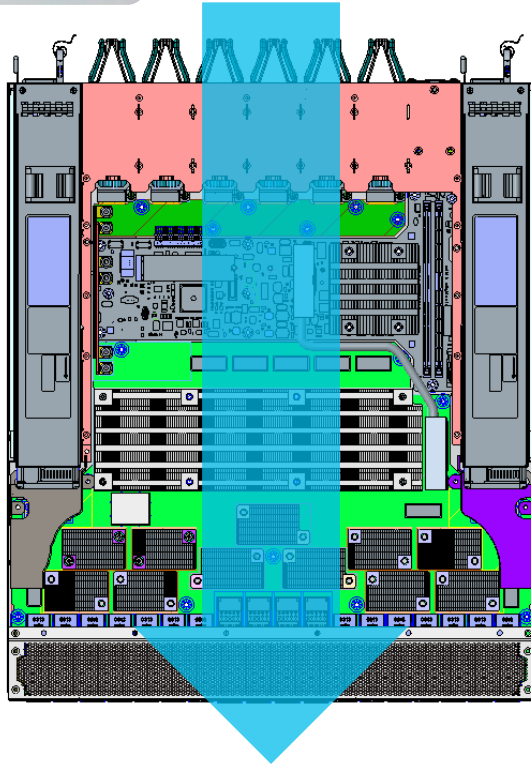
PSU2

- Mix of AC and DC power supplies supported

Catalyst 9500X – reversible airflow



Back to front
Port-side exhaust

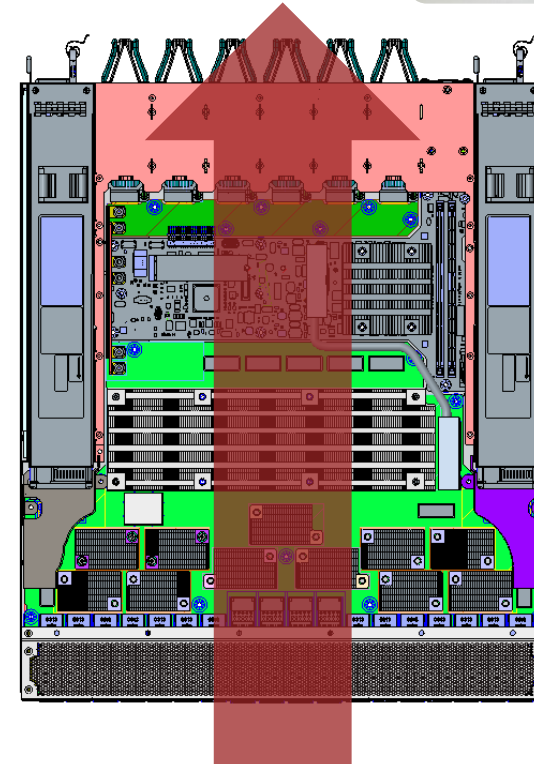


- Color of fan unit handle/latch represents direction of airflow
- Different fan product IDs for different airflow directions
 - **Royal blue** – back to front
 - **Burgundy** – front to back
- All fans must be the same color (direction) to work correctly



Single **1500W AC/DC PSU**
with **Cisco Grey** latch
for both airflow directions

Front to back
Port-side intake



Same power supply and fan tray unit compatible with both C9500X-28C8D and C9500X-60L4D switches

SDM Templates

Supported on 9500X and 9500 High Performance Models

Cisco Catalyst 9500 Series

Switch Database Management (SDM) template

Core template

Maximizes system resources for unicast and multicast routing and security
(Default: Cisco Catalyst 9500 Series High Performance Switches)

SD-Access template

Maximizes system resources for security to support fabric deployment

User-customizable template

Allows customizable*
ACL and FIB TCAM resources



Cisco® Catalyst®
9500 Series

Distribution template

Maximizes system resources for MAC and security
(Default: Cisco Catalyst 9500 Series Switches)

NAT template

Maximizes the Network Address Translation (NAT) configurations on the switch

* Cisco Catalyst 9500 Series High Performance switch only.

Cisco Catalyst 9500 Series

SDM templates and scale numbers

Feature		Distribution template (default)	Core template	SD-Access template	NAT template
Indirect/LPM routes (IPv4/IPv6)		64,000/32,000	64,000/32,000	64,000/32,000	64,000/32,000
Direct/host routes (IPv4/IPv6)		48,000/24,000	32,000/16,000	80,000/40,000	48,000/24,000
Multicast routes (IPv4/IPv6)		16,000/8000	16,000/8000	16,000/8000	16,000/8000
MAC address table		64,000	16,000	16,000	16,000
Flexible NetFlow		128,000 per ASIC	128,000 per ASIC	128,000 per ASIC	128,000 per ASIC
SGT labels		8000	8000	8000	8000
Security ACLs	Ingress	18,000			18,000
	Egress				
QoS ACLs	Ingress	18,000			3000
	Egress				
NetFlow ACLs	Ingress	1000			1000
	Egress	2000			2000
SPAN	Ingress	1000			1000
	Egress				
PBR/NAT		2000			16,000
CoPP		1000			1000
Tunnel termination and MACsec		1000			1000
LISP		1000			1000

Cisco Catalyst 9500H Series

SDM templates and scale numbers

IOSXE 17.2.x or earlier

Feature		Distribution	Core (default)	SDA	NAT
Routes (IPv4/IPv6)		114K/114K	212K/212K	212K/212K	212K/212K
Multicast routes (IPv4/IPv6)		16K/16K	32K/32K	32K/32K	32K/32K
MAC address table		82K	32K	32K	32K
IGMP/MLD snooping		2K	2K	2K	2K
Flexible NetFlow (Ingress)		49K/ASIC	32K/ASIC	32K/ASIC	32K/ASIC
Flexible NetFlow (Egress)		49K/ASIC	32K/ASIC	32K/ASIC	32K/ASIC
SGT label		32K	32K	32K	32K
Security ACL	Ingress 		12K	8K	12K
	Egress 		15K	19K	8K
QOS ACL	Ingress 		8K	8K	4K
	Egress 		8K	8K	4K
NetFlow ACL	Ingress 		1K	1K	1K
	Egress 		1K	1K	1K
SPAN	Ingress 		0.5K	0.5K	0.5K
	Egress 		0.5K	0.5K	0.5K
PBR/NAT			3K	2K	15.5K
CPP			1K	1K	1K
Tunnel termination and MACsec			3K	3K	2K
LISP			1K	2K	1K

 Customizable resources

Cisco Catalyst 9500H & 9600 Series

SDM templates and scale numbers

IOSXE 17.3.1

Feature		Distribution	Core (default)	SDA	NAT
	Routes (IPv4/IPv6)	114K/114K	212K/212K	212K/212K	212K/212K
	Multicast routes (IPv4/IPv6)	16K/16K	32K/32K	32K/32K	32K/32K
	MAC address table	82K	32K	32K	32K
	IGMP/MLD snooping	2K	2K	2K	2K
	Flexible NetFlow (Ingress)	48K/ASIC	32K/ASIC	32K/ASIC	32K/ASIC
	Flexible NetFlow (Egress)	48K/ASIC	32K/ASIC	32K/ASIC	32K/ASIC
	SGT/MPLS label	32K	32K	32K	32K
Security ACL	Ingress 	12K		8K	12K
	Egress 	15K		19K	8K
QOS ACL	Ingress 	8K		8K	4K
	Egress 	8K		8K	4K
NetFlow ACL	Ingress 	1K		1K	1K
	Egress 	1K		1K	1K
SPAN	Ingress 	0.5K		0.5K	0.5K
	Egress 	0.5K		0.5K	0.5K
PBR/NAT		3K		2K	15.5K
CPP		1K		1K	1K
Tunnel termination and MACsec		3K		3K	2K
LISP		1K		2K	1K

Higher scale

 Customizable resources

FIB Scale Customization

* Total Multicast (L2+L3) =/ < 48K

Feature	Scale Values (Min – Max)	Default Value	Step Units
L2 MAC	32K – 128K	32K	16K
L3 Unicast	64K – 256K	64K	16K
L3 Multicast *	0 - 32K	16K	16k
L2 Multicast *	0 - 32K	16K	16K
SGT & MPLS IP-to-Tag labels	0 - 64K	32K	32K
Netflow - Input	0 - 64K	32K	32K
Netflow - Output	0 - 64K	0	32K
Total Resources	416K		

Scale Values: minimum and maximum possible values
Step Units: granularity (block size) of scale per type
Default Value: default value, if it's not specified by CLI

16K – 16384
 32K – 32768

FIB Allocation Examples

* Netflow requires 2X for flow records

Feature	Customer 1 (L2 focus)	Customer 2 (L3 focus)	Customer 3 (FNF focus) *
L2 MAC	128K	32K	32K
L3 Unicast	144K	256K	64K
L3 Multicast	32K	16K	16K
L2 Multicast	16K	32K	16K
SGT & MPLS IP-to-Tag labels	64K	64K	32K
Netflow - Input	32K	32K	64K *
Netflow - Output	0	0	64K *
Total Resources	416K		

16K – 16384

32K – 32768

Cisco Catalyst 9600 & 9500H Series

SDM Templates, Scale & Customization

New - IOSXE 17.4.1

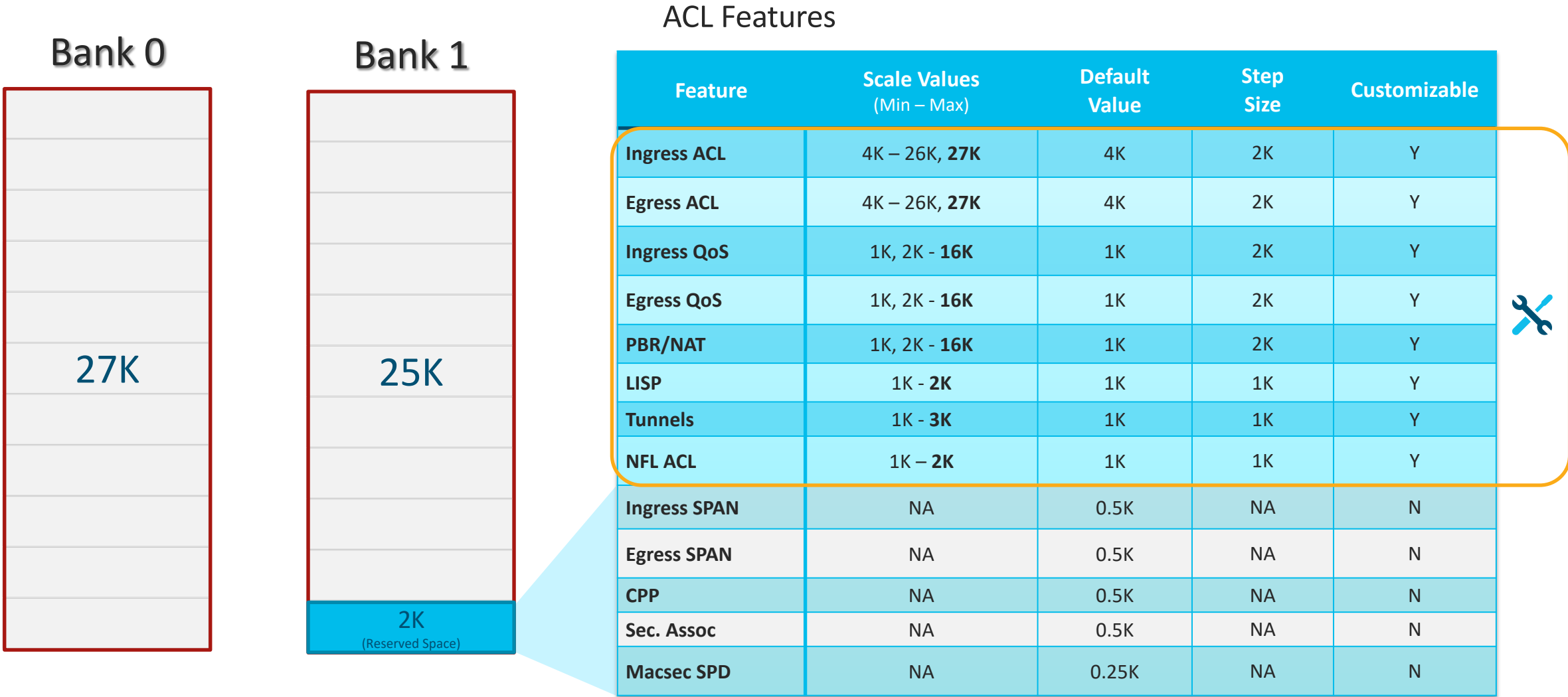
Feature		Distribution	Core (default)	SDA	NAT
	Routes (IPv4/IPv6)	114K/114K	212K/212K	212K/212K	212K/212K
	Multicast routes (IPv4/IPv6)	16K/16K	32K/32K	32K/32K	32K/32K
	MAC address table	82K	32K	32K	32K
	IGMP/MLD snooping	2K	2K	2K	2K
	Flexible NetFlow (Ingress)	49K/ASIC	32K/ASIC	32K/ASIC	32K/ASIC
	Flexible NetFlow (Egress)	49K/ASIC	32K/ASIC	32K/ASIC	32K/ASIC
	SGT label	32K	32K	32K	32K
	Security ACL	Ingress	12K	8K	12K
		Egress	15K	19K	8K
	QOS ACL	Ingress	8K	8K	4K
		Egress	8K	8K	4K
	NetFlow ACL	Ingress	1K	1K	1K
		Egress	1K	1K	1K
	SPAN	Ingress	0.5K	0.5K	0.5K
		Egress	0.5K	0.5K	0.5K
	PBR/NAT		3K	2K	15.5K
	CPP		1K	1K	1K
Tunnel termination and MACsec			3K	3K	2K
LISP			1K	2K	1K

Higher scale

 Customizable resources

ACL Scale Considerations

New - IOSXE 17.4.1



ACL Allocation Examples

* 2K entries are reserved for System

Feature *	Customer 1 (Security focus)	Customer 2 (QoS focus)	Customer 3 (NAT focus)
Security - Input	27K	6K	12K
Security - Output	18K	6K	8K
QoS - Input	1K	16K	6K
QoS - Output	1K	16K	4K
PBR/NAT	2K	3K	16K
LISP	1K	2K	2K
Tunnels	1K	2K	1K
Netflow ACL	1K	1K	1K
Total Resources *	54K		

1K - 1024
16K – 16384

Cisco Catalyst 9500X

Switch Database Management (SDM) template

Default template

Maximizes system resources
for Layer 3 unicast and
multicast **routes**

User-customizable template

Allows customizable
ACL TCAM resources



Cisco® Catalyst®
9600 Series

Custom template

Provide flexibility for
customizing TCAM space for
specific requirements



Silicon One Q200 SDM template – 17.7.1

Features	Customizable	DEFAULT (core + edge)	Custom (min to max @ step)	
MAC addresses	✓	128,000	32,000 to 256,000	@ 1000 step
Host routes (ARP/NDP)	✓	128,000/64,000	32,000 to 256,000	@ 1000 step
Layer 2 multicast entries (IGMP/MLD)	FCS+	16,000/8000	0 to 64,000	@ 1000 step
Layer 3 multicast routes (IPv4/IPv6)	FCS+	32,000/16,000	0 to 64,000	@ 1000 step
ACL compression (SGT, DGT, OGID/v6)	✓	32,000/16,000	0 to 64,000	@ 1000 step
MPLS labels	✓	256,000	0 to 512,000	@ 1000 step
Reserved (PBR/NAT)	FCS+	16,000/8,000	0 to 256,000	@ 1000 step
	CEM	608,000 (288,000 for LPM)		
Layer 3 unicast routes (IPv4/IPv6)	FCS+	2 million/ 1 million	1 million to 2 million	@ 1 million step
Features	Customizable	DEFAULT (core + edge)	Custom (min to max @ step)	
Security ACL (IPv4/IPv6)	FCS+	8000/4000 shared*	0 to 11,000/5000	@ 1 step
Quality of service (IPv4/IPv6)	FCS+	8000/4000 shared*	0 to 11,000/5000	@ 1 step
Policy-based routing (IPv4/IPv6)	FCS+	8000/4000 shared*	0 to 11,000/5000	@ 1 step
Lawful intercept (IPv4/IPv6)	FCS+	1000 (2x 512) reserved	1000 to 5000/2500	@ 1 tap (2 ACE)
LPTS, EPC, FSPAN, NFL (IPv4/IPv6)	FCS+	1000 (2x 512) reserved	1000	@ 1 step
	TCAM	10,000 (2000 for LPM)		

* Shared is an unreserved space, first come, first served per feature.

FIB Allocation Examples

Feature	Customer 1 (L2 focus)	Customer 2 (L3 focus)
MAC addresses	256K	32K
Host routes (ARP/NDP)	32K	256K
Layer 2 multicast entries (IGMP/MLD)	64K	16K
Layer 3 multicast routes (IPv4/IPv6)	16K	64K
ACL compression (SGT, DGT, OGID/v6)	64K	64K
MPLS labels	32K	512K
Reserved (PBR/NAT)	0	0
Total Resources	608K	
Layer 3 unicast routes (IPv4/IPv6)*	1M/500K	2M/1M

*Roadmap

16K – 16384
32K – 32768

Cisco Unified Access Data Plane (UADP) Architecture

Applicable to 9500 High Performance Models

UADP 3.0



~20B transistors
16-nm technology



Customizable ASIC
templates



36-MB
unified buffer



Double-width tables



3x more FIB scale



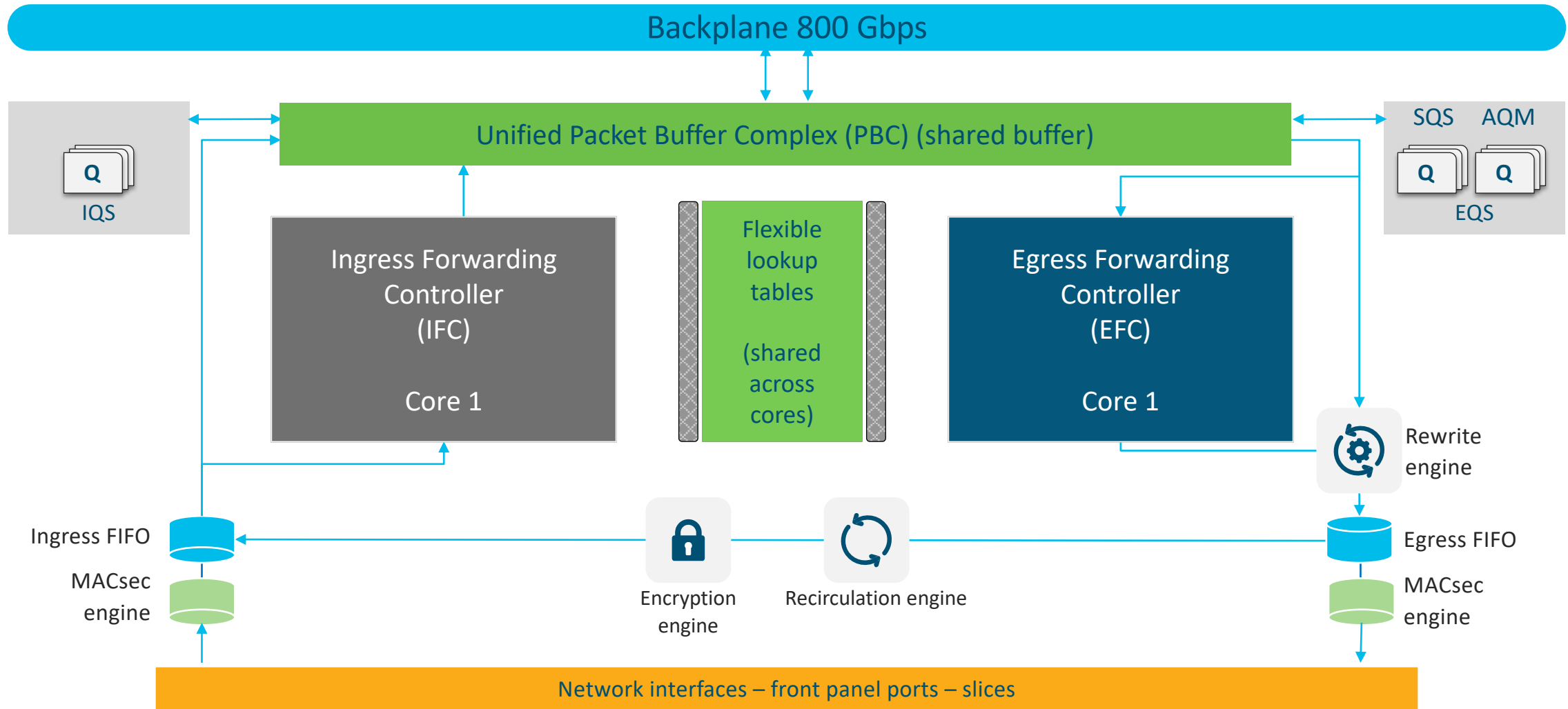
Up to 1.6 TB
bandwidth



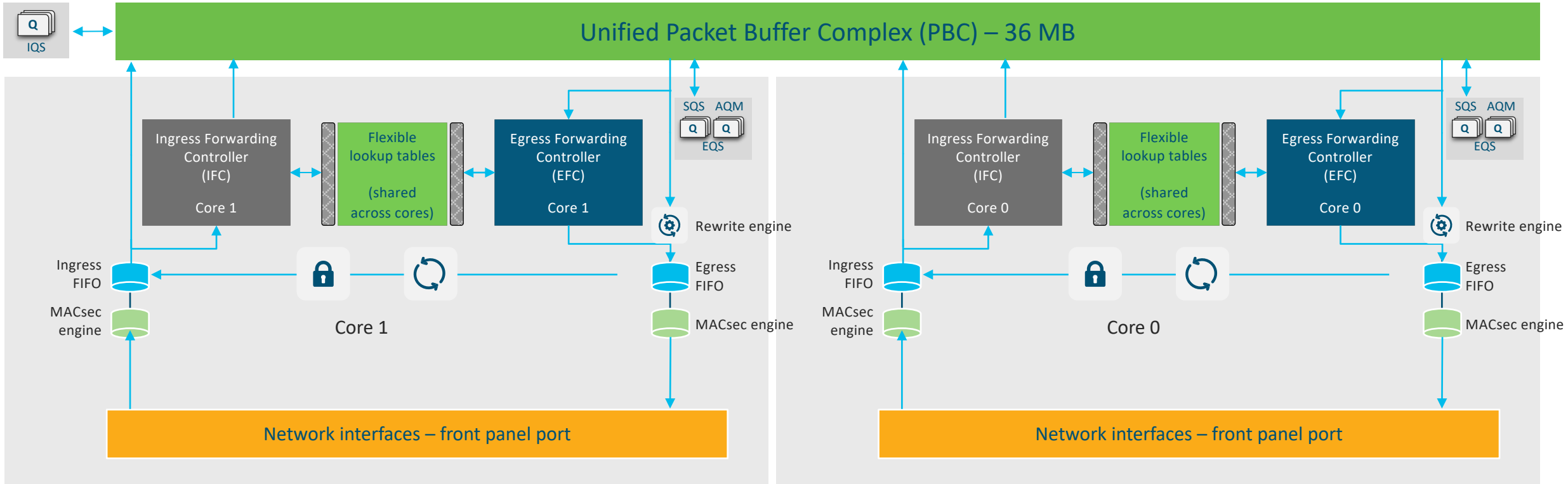
1G, 10G, 20G,
25G, 40G, and 100G
speeds

Cisco Catalyst 9500 Series

UADP 3.0 – under the covers

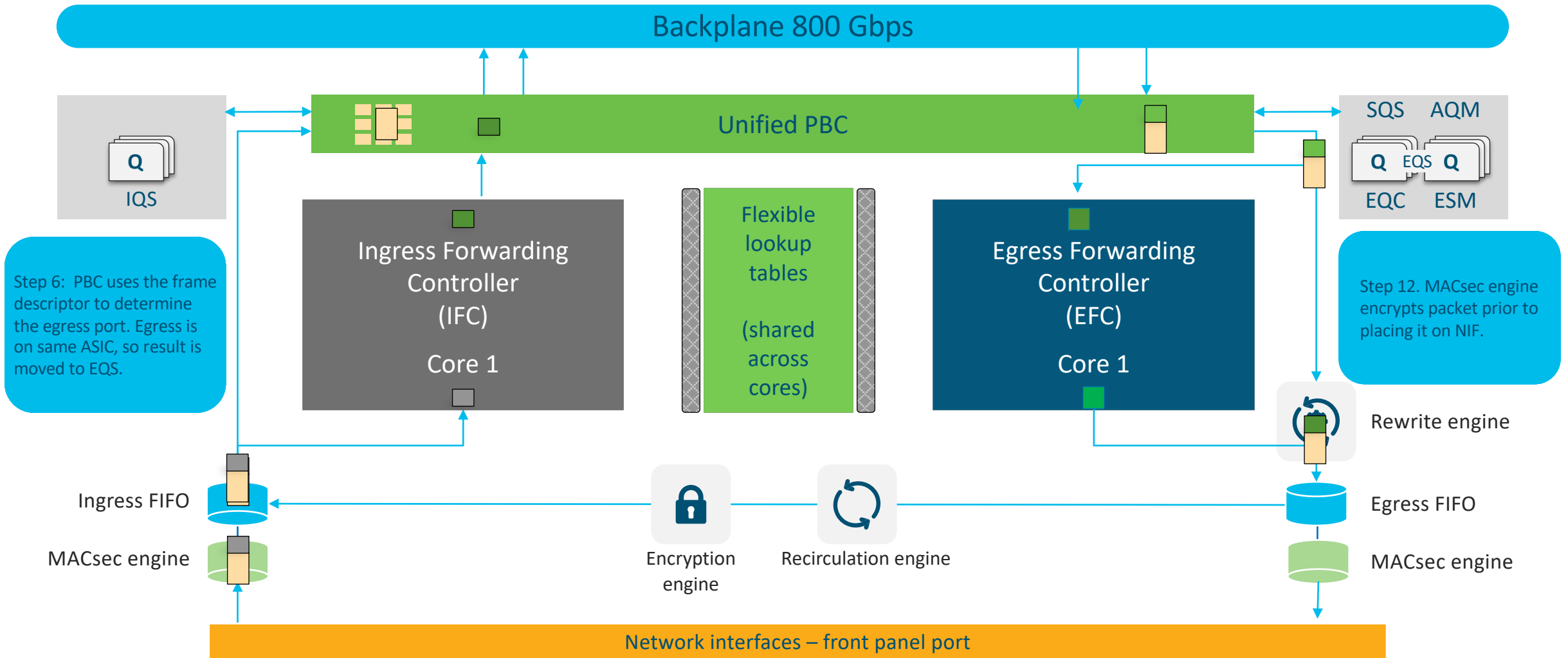


UADP 3.0 – under the covers



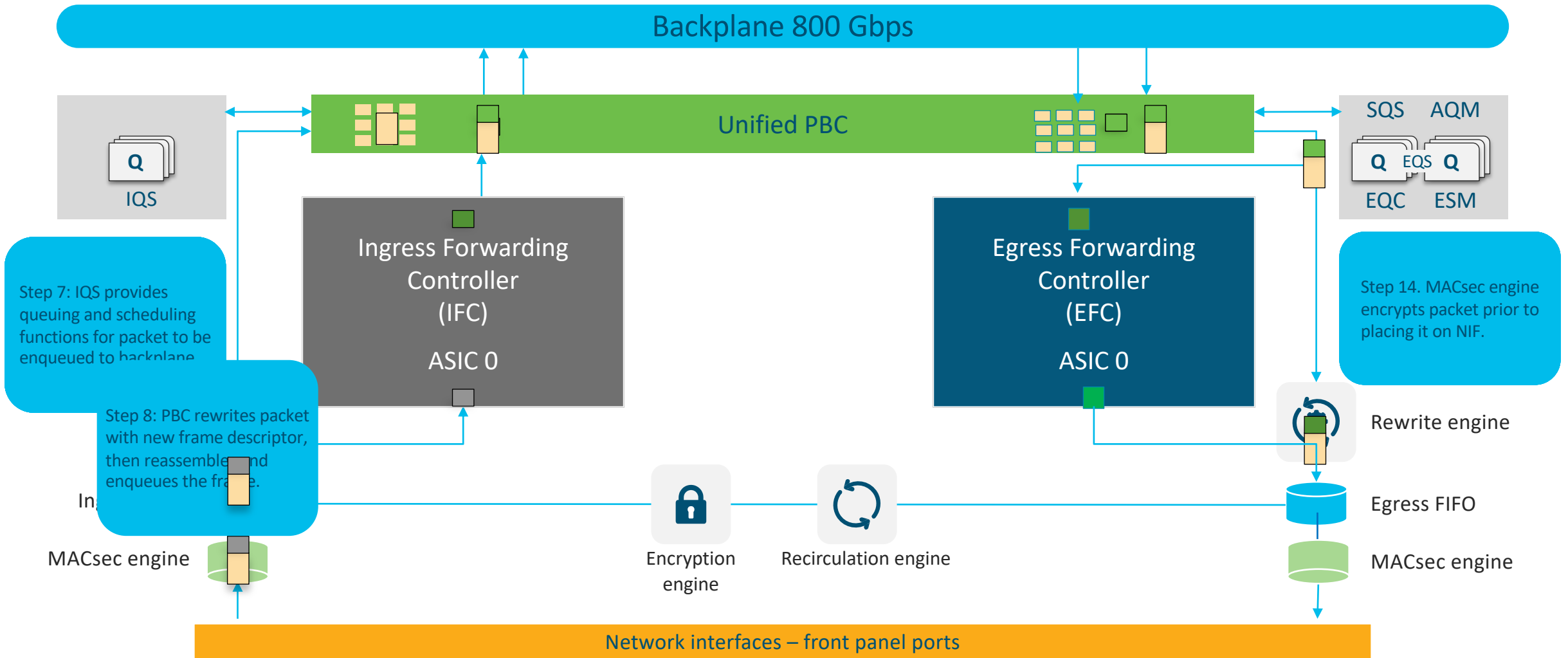
Cisco Catalyst 9500 Series

Unicast forwarding within ASIC (ingress and egress)



Cisco Catalyst 9500 Series

Unicast forwarding across ASIC (ingress and egress)



Cisco Catalyst 9500 Series ASIC comparison

 Capabilities (per ASIC)	Cisco® Catalyst® 9500 Series (UADP 2.0)	Cisco Catalyst 9500 Series High Performance (UADP 3.0)
Switching and forwarding capacity	240 Gbps/360 Mpps	1.6 Tbps/1 Bpps
Stack bandwidth	2x 360 Gbps	2x 400 Gbps
Buffer capability	2x 16 MB	36 MB shared buffer
Switch Database Management (SDM) template	Fixed templates	Customizable templates
NetFlow capabilities	Dedicated NetFlow table	Shared NetFlow table
v4 FIB scale	Total 228,000*	Total 412,000*
v4 and v6 scale	v6 reduced by half	v4 and v6 same scale

* Maximum ASIC capability.

Cisco Catalyst 9500 Series Switches scale comparison

Model	C9500-16X	C9500-40X	C9500-12Q	C9500-24Q	C9500-32C	C9500-32QC	C9500-48Y4C, C9500-24Y4C	C9500X-28C8D
Switching capacity	240G	480G	480G	960G	3.2T	1.6T	1.6T	6T
Forwarding rate	320 Mpps	720 Mpps	720 Mpps	1440 Mpps	2 Bpps	1 Bpps	1 Bpps	8 Bpps
MAC addresses	64,000*	64,000*	64,000*	64,000*	82,000*	82,000*	82,000*	256,000
LPM/host routes (IPv4/v6 routes)	64,000/32,000* 32,000/16,000	64,000/32,000 * 32,000/16,000	64,000/32,000* 32,000/16,000	64,000/32,000* 32,000/16,000	212,000/ 212,000*	212,000/ 212,000*	212,000/ 212,000*	2M
Multicast routes	48,000*	48,000*	48,000*	48,000*	32,000*	32,000*	32,000*	64,000
Security ACLs	18,000*	18,000*	18,000*	18,000*	27,000*	27,000*	27,000*	12,000
QoS ACLs	18,000*	18,000*	18,000*	18,000*	16,000*	16,000*	16,000*	12,000
Flexible NetFlow	128,000 per ASIC	128,000 per ASIC	128,000 per ASIC	128,000 per ASIC	96,000*	96,000*	96,000*	2M Sampled
Spanning Tree instances**	256	256	256	256	1000	1000	1000	4000

* Depends on SDM template.

** For 16.11.1 release.

Cisco Silicon One (S1) Q200 Architecture

Applicable to 9500X-28C8D Switch



Introducing Cisco Silicon One

One architecture, multiple devices



Q202

3.2 Tbps



Q201

6.4 Tbps



Q100

10.8 Tbps



Q200

12.8 Tbps

- First network silicon to break the 10-Tbps barrier
- Comprehensive routing, with switching efficiency
- **Flexible P4 NPL programmable packet processing**

- Multiple functions: System-on-chip, line card, or fabric
- Multiple form factors: Fixed or modular
- **Multiple segments: Enterprise and service provider**

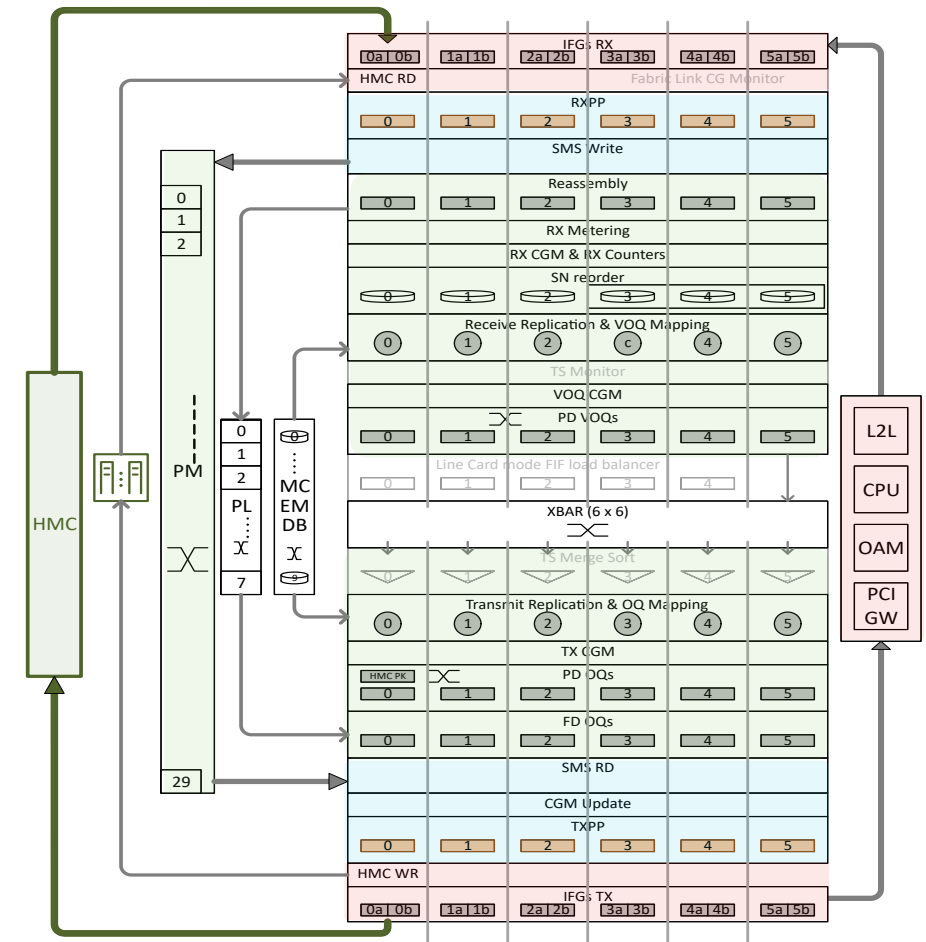
www.cisco.com/c/en/us/solutions/service-provider/innovation/silicon-one.html

Cisco Silicon One Q200

Programmable next-generation ASIC

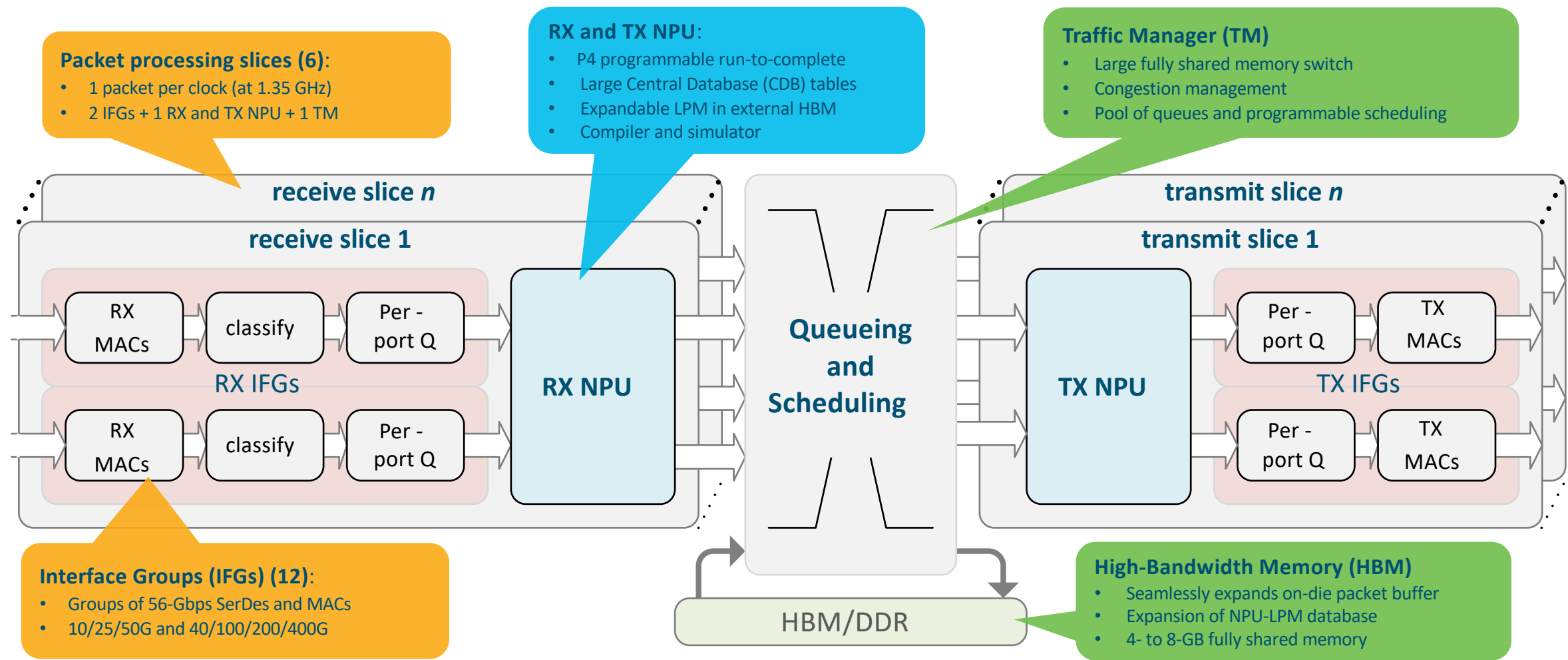


- **Generation 1.1, 7-nm ASIC**
- **6 slices** for **≤8.1 Bpps** throughput
- **12.8-Tbps** bandwidth at **1.35 GHz**
- **256 SerDes** at **56G PAM4**
- **~80-MB internal buffer** (up to 8-GB HBM)
- **~2 million internal Longest Prefix Match (LPM) routes** (up to 4 million in HBM)
- **~608,000 shared CEM** (896,000, with 288,000 for LPM)
- **~10,000 shared TCAM entries** (96,000/6, with 16,000 for LPM)





Silicon One ASIC architecture overview





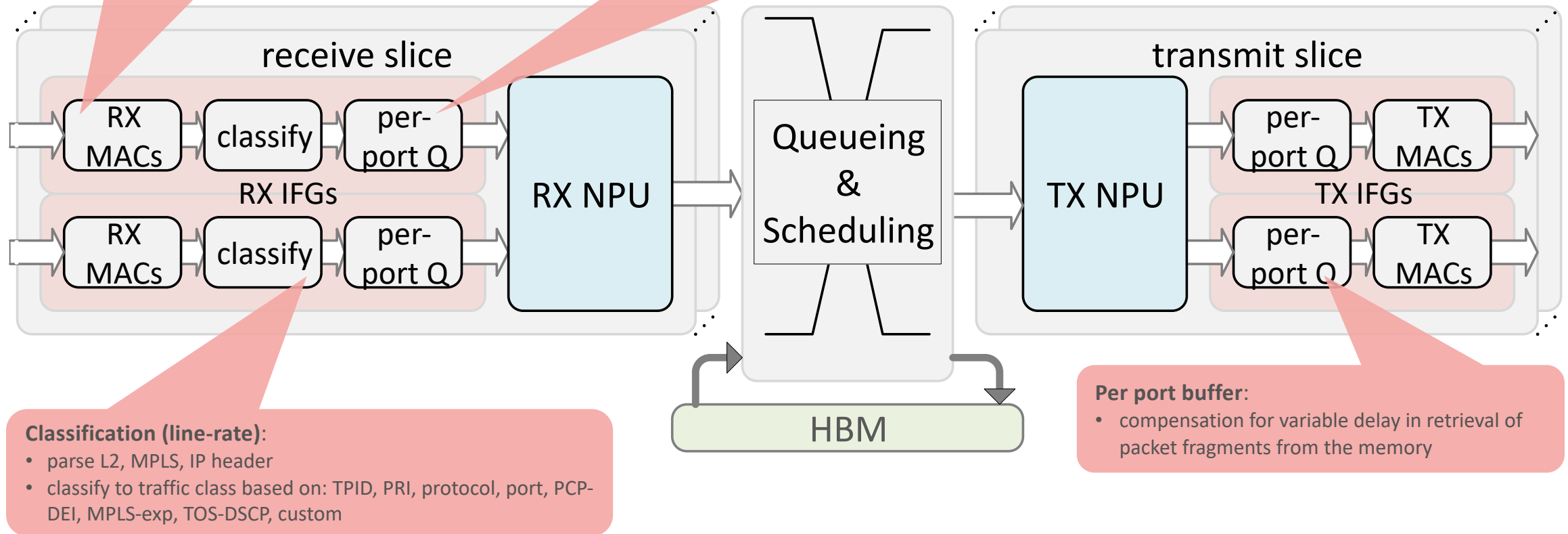
S1- Interface Groups (IFG) Overview

Interface Groups (IFGs):

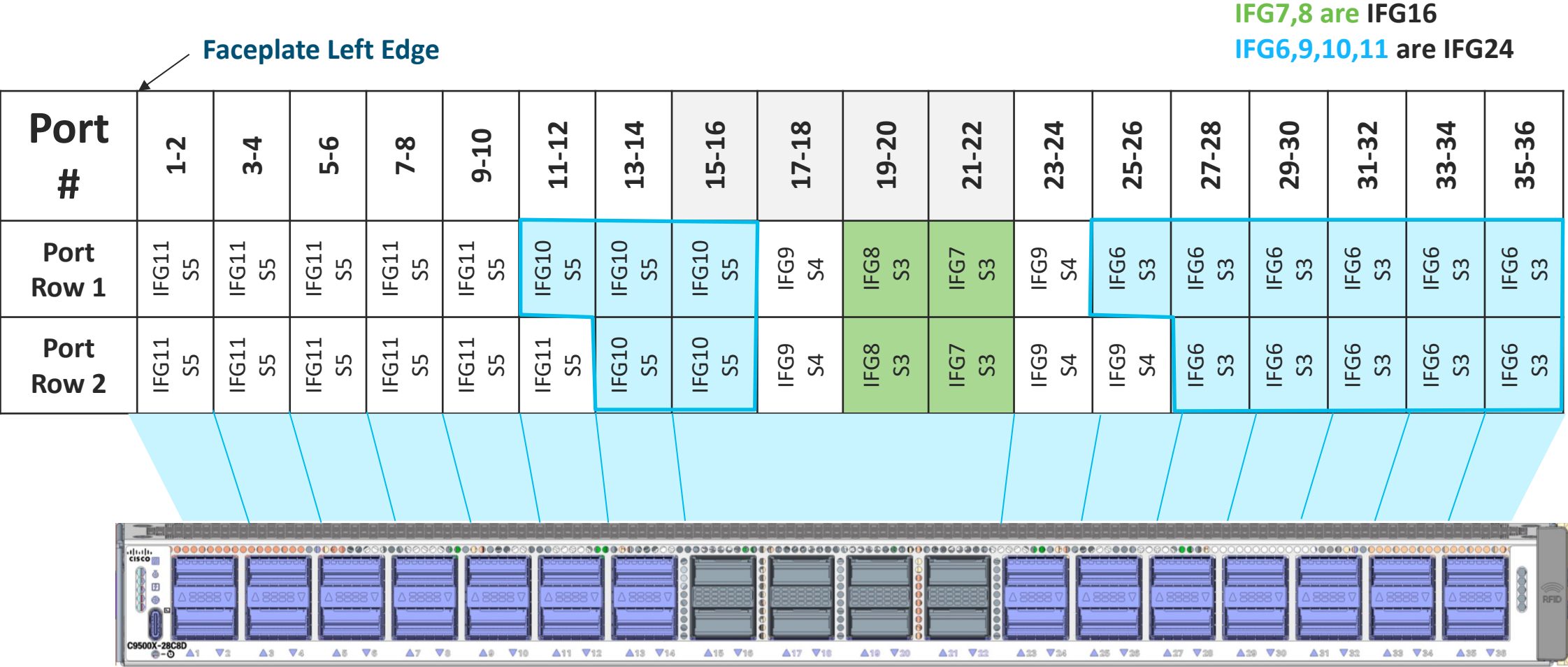
- pool of 56Gbps SerDes & MACs
- 10/25/50GE or 40/100/200/400GE
- Q200 (Gibraltar) – 256 total SerDes

Per port buffer:

- admission test based on Traffic Class
- absorb/smooth temporary burst oversubscription
- flow-control generation for lossless to core
- 4Mb – partitioned between ports



Startrek Farscape - GB IFG#, Slice# Map





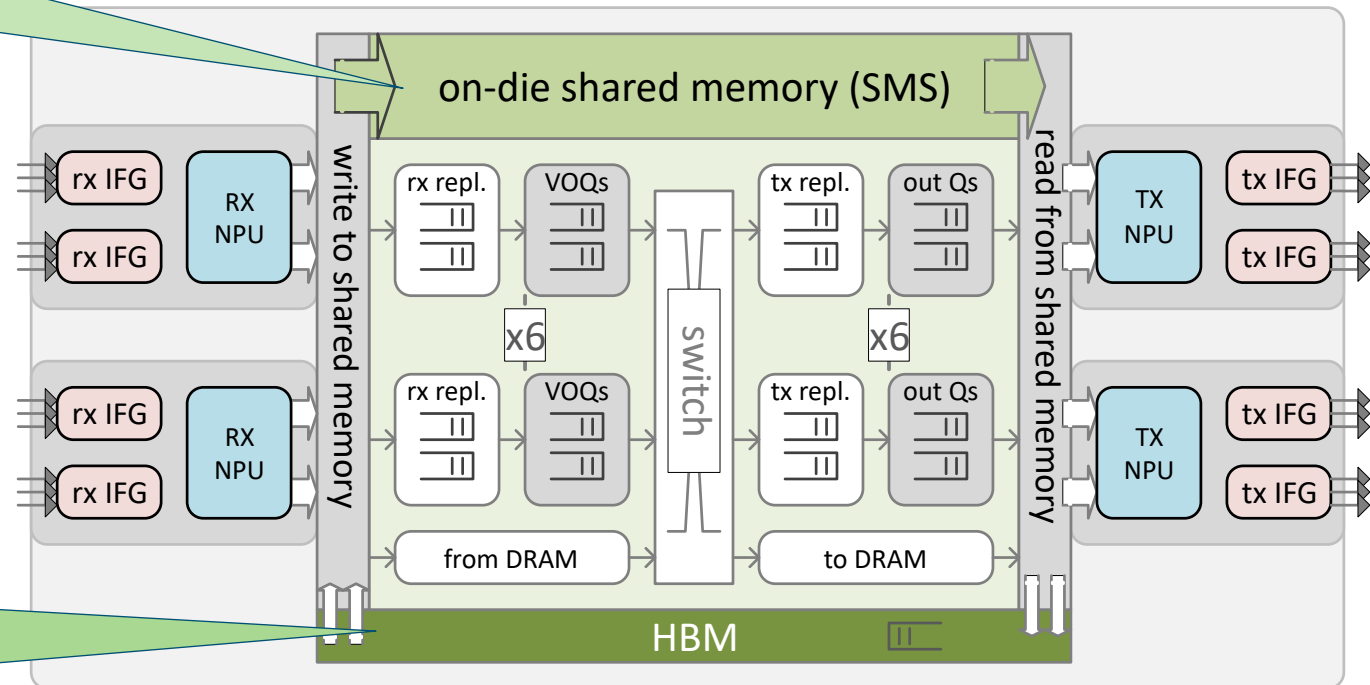
S1 – Buffer Queuing Overview

Onboard SMS vs. HBM

Shared Memory Subsystem (SMS)

- Fully shared across slices:
- 14 x 128B write + 14 x 128B read buses
- **108MB** managed as **288K** x 384B buffers
- multicast buffering – write once, read many

~12.8T bps = ~8.1B packets-per-second (6 x 1.35GHz)



High Bandwidth Memory (HBM)

- fully shared across slices
- 2 x 128B write + 2 x 128B read buses
- ~2Tbps full-duplex (in and out)
- **8GB** managed as 1M x 8KB buffers
- DRAM packets – combine up to 32 small packets

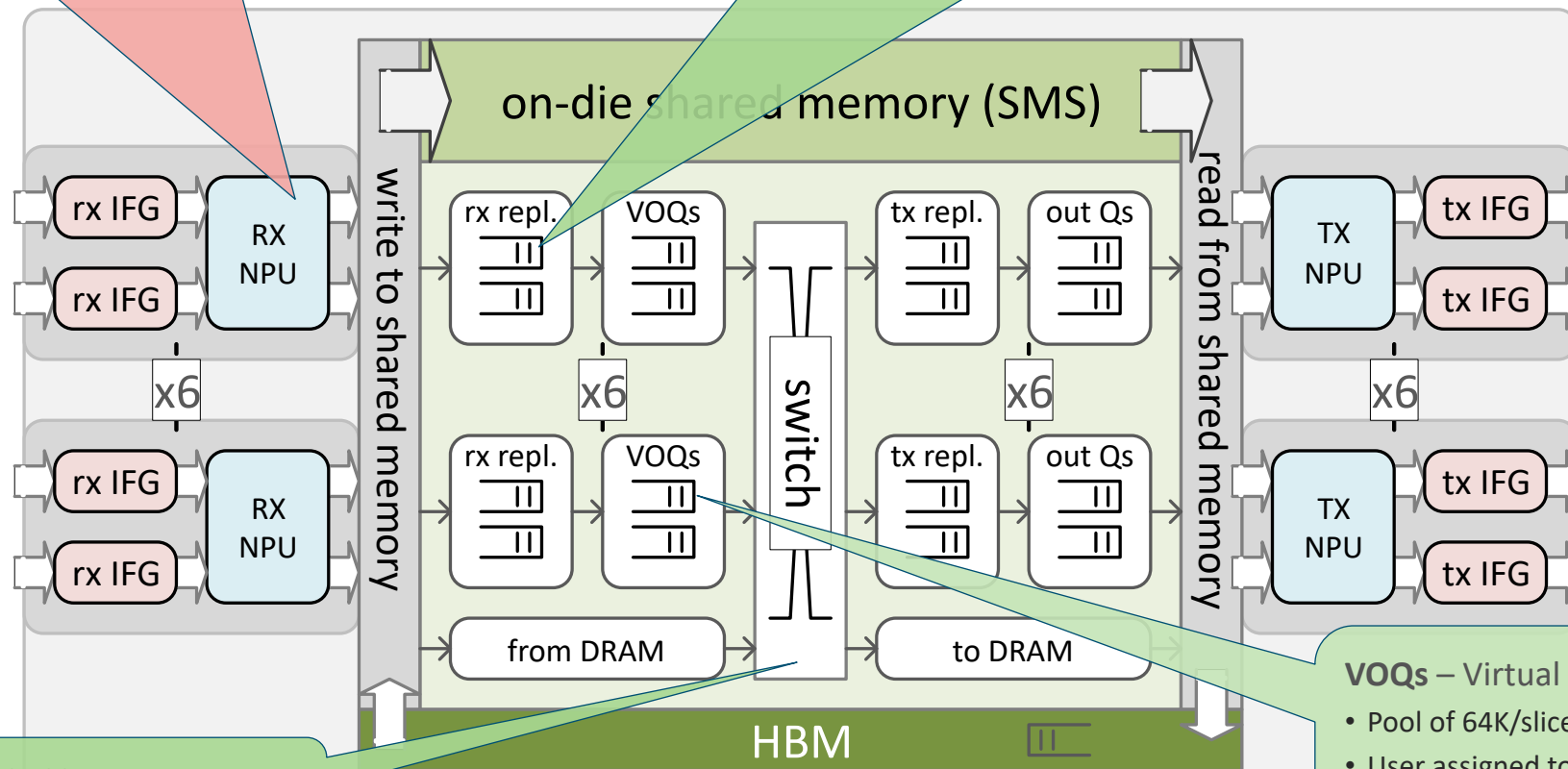
S1 Queuing – Ingress Queues

IFG RXQ – Interface-Group Receive-Queue

- Buffer data (FIFO) received from the various Ethernet ports, before injection into the core

RXRQ – Receive Replication-Queues

- Store PDs of multicast packets that require replication, before VOQs



PDSQ – PD Switch-Queues

- queue per crosspoint (mesh) of the switch

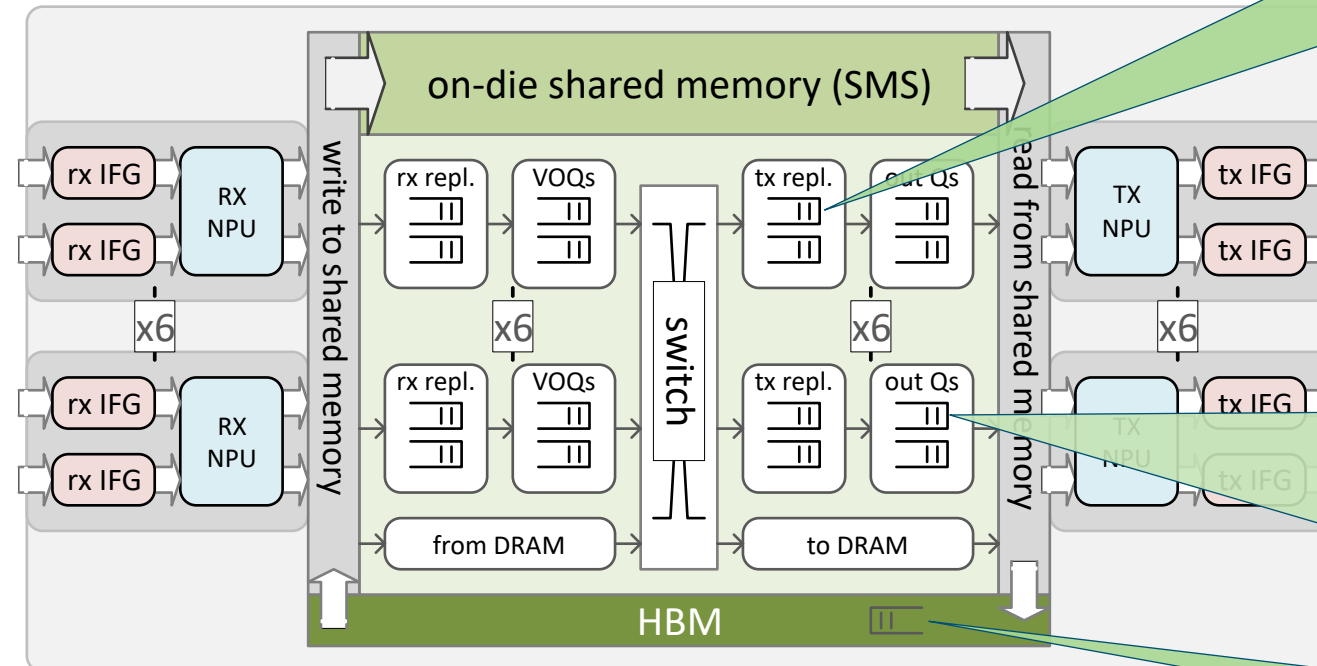
VOQs – Virtual Output Queues

- Pool of 64K/slice of Queues
- User assigned to a OQ or TXRQ
- Seamlessly extendable in HBM

S1 Queuing – Egress Queues

TXRQs – Transmit Replication Queues

- store descriptors of packets that need to be replicated



OQs – Output Queues

- store packets per transmit interface (Ethernet, Hosts, Recycle)
- each OQ is a pair (one unicast + one multicast)
 - unicast – stores packets received in return for credits
 - multicast – stores packets replicated at TX replicator
- 208 OQ (pairs) per IFG16/24
- grouped in 8x OQ or 2x OQ per system-port
- OQ-Group is a shaping & scheduling group, assigned to a transmit interface (corresponding to a System Port)

DRAM-Q

- extend the VOQ pools to HBM (DRAM)
- pool of queues are dynamically assigned to VOQs

Platform Comparison

Catalyst 9500X

Port Density

	 Catalyst® 9500X-28C8D	 Catalyst 9500X-60L4D	 Catalyst 9500-48Y4C			
	S1 Family		UADP Family			
CPU (BDW-NS, BDW)	2.7 GHz 8C Intel® (BDW-NS)	2.7 GHz 8C Intel® (BDW-NS)	2.4 GHz 4C Intel® (BDW-NS)			
DRAM (type)	32 GB (DDR4)	32 GB (DDR4)	16 GB (DDR4)			
ASIC (number)	Q200 (1x)	Q200 (1x)	UADP 3.0 (1x)			
Capacity	12 Tbps (full duplex)	9.2 Tbps (full duplex)	3.2 Tbps (full duplex)			
	No Breakout	With Breakout	No Breakout	With Breakout	No Breakout	With Breakout
10G max	36 with QSA	88	60 Native + 4 QSA	76*	48 Native + 4 QSA	64
25G max	-	88	60	76*	48	64
50G max	-	88	60	76*	-	
40G max	36	60*	4	16*	4	
100G max	36	60	4	16*	4	
400G max	8		4		-	
Encryption	MACsec and WAN-MACsec		IPsec*, WAN-MACsec and MACsec		MACsec	

* Roadmap (not committed)

Catalyst 9500X and 9500H – features and scales

	 Catalyst® 9500X (Silicon One™ Q200)		 Catalyst 9500H (UADP 3)	
	Default	Maximum ^(Custom)	Default	Maximum ^(custom)
MAC addresses	128,000	256,000	80,000	128,000
IP host routes	128,000	256,000	80,000	128,000
Multicast L2 groups	16,000	64,000*	16,000	48,000
Multicast L3 routes	32,000	64,000*	32,000	48,000
IP LPM routes	2 million	2 million	212,000	256,000
MPLS labels	256,000	512,000	32,000	64,000
SGT/OG labels	32,000	64,000	32,000	64,000
NAT* sessions	16,000*	128,000*	3000	16,000
Security ACL entries	8000	10,000*	12,000	27,000
QoS ACL entries	8000	10,000*	8000	21,000
PBR* ACL entries	8000*	10,000*	3000	16,000

* Roadmap for Catalyst 9600X (not committed).

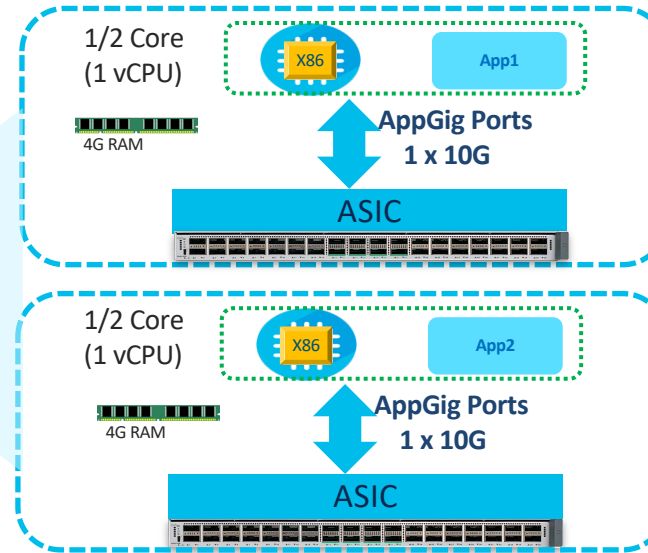
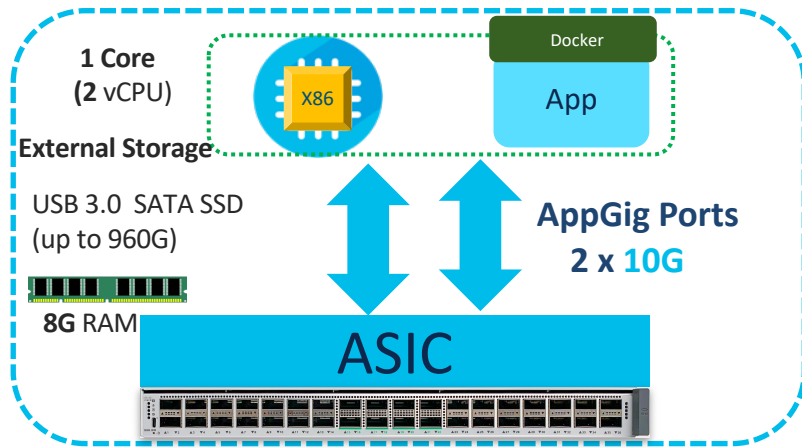
C9500X and C6K Sup2T/6T XL Scale

Model	C9500X	C9500H	C6K-Sup720 3C	C6K-Sup2T	C6K-Sup6T
Switching capacity	12.8T	9.6T	720G	2T	6T
Forwarding rate (IPv4/IPv6)	8 Bpps 8 Bpps	3 Bpps 3 Bpps	450Mpps 225Mpps	720Mpps 390Mpps	780Mpps 390Mpps
MAC addresses	256,000*	82,000*	96,000	128,000	128,000
LPM/host routes (IPv4/IPv6)	2,000,000* 1,000,000*	212,000* 212,000*	1,000,000 500,000	1,000,000 500,000	1,000,000 500,000
Multicast routes	32,000*	32,000*	32,000	128,000	128,000
Security ACLs	10,000*	27,000*	Dedicated 32,000	Shared with QoS 256,000	Shared with QoS 256,000
QOS ACLs	10,000*	16,000*	Dedicated 32,000	Shared with Security 256,000	Shared with Security 256,000
Flexible NetFlow	2,000,000 (Sampled)	96,000*	256,000/ASIC	1,000,000/ASIC	1,000,000/ASIC
VLAN ID	4,000	4,000	4,000	4,000	4,000
Spanning Tree instances	4,000	4,000*	4,000	4,000	4,000

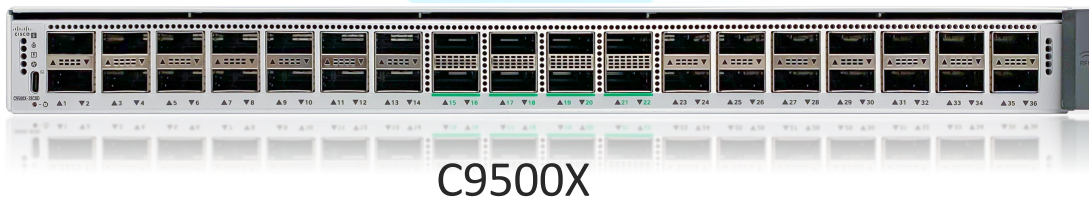
* Depends on SDM customization

Application Hosting

Application Hosting Infrastructure on C9500X



2X Cisco Signed Applications

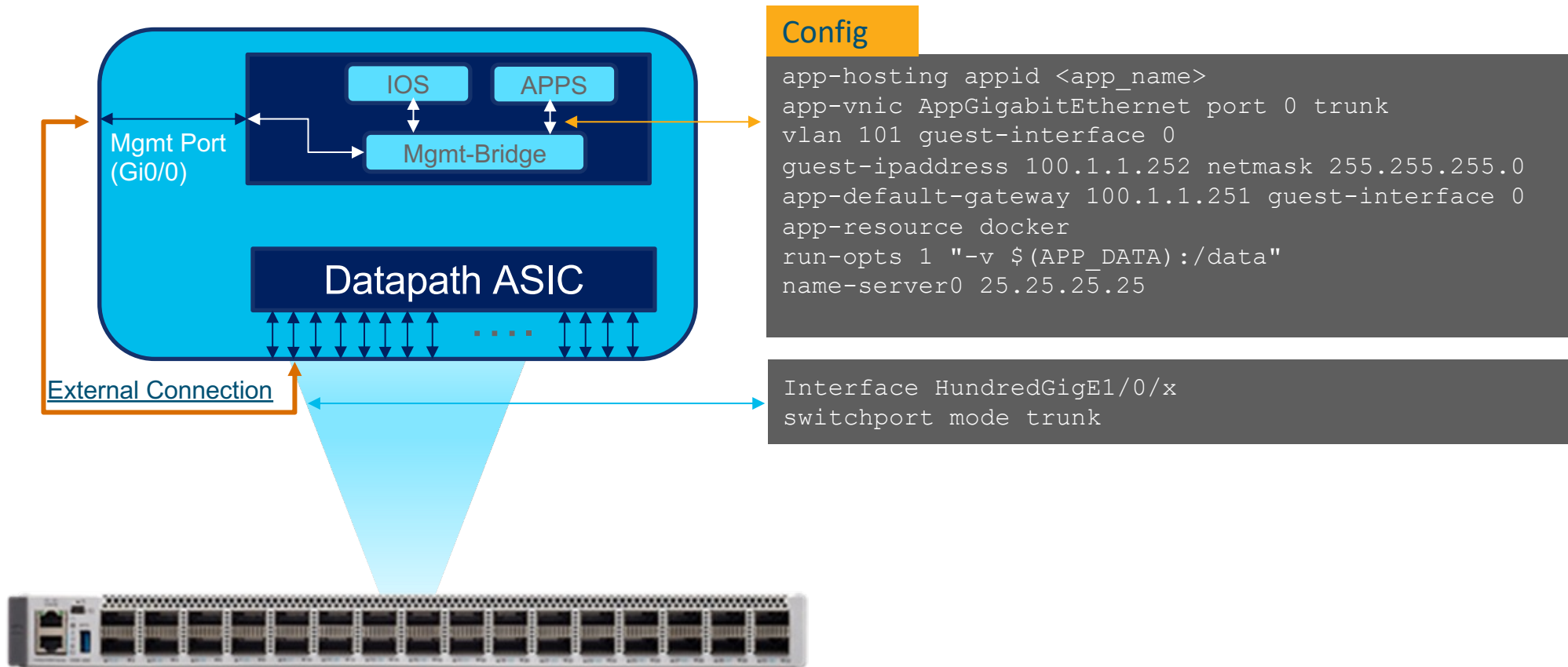


Support for Multiple Docker applications
With Additional RAM Memory and 2 x AppGigabit Ports, multiple Cisco Signed performance savvy Applications can be hosted on C9500X

Application Hosting on C9500H

Using Front Panel Port

IOS-XE 17.5.1





Competitive information

Catalyst 9500X for continued market leadership

Competitive challenges

ARISTA



Campus: 7050SX3



Data center: 7280R3

aruba
a Hewlett Packard
Enterprise company



CX 8320/25



CX 8360

Threats

- 7050SX3 in campus with higher 40/100G density
- Positioning data center switch: 7280R3 in campus core with higher scale and speeds/feeds

Threats

- Higher port densities
- Higher route, MAC scales

Leadership with Catalyst® 9500X and 9500 models

	Cisco Catalyst 9500X	Arista 7280R3	Cisco Catalyst 9500H	7050SX3	Aruba CX8300
	Q200	Jericho2	UADP	Trident3	T3/Gen 7
Scale, performance, hardware differentiation					
More IP LPM routes	Best	Best	Partial	Partial	Partial
Scaled MPLS labels	Best	Best	Partial	Bad	Bad
Extensive security, QoS, PBR ACLs	Best	Best	Partial	Bad	Partial
400G ports	Best	Best	Bad	Bad	Bad
Customizable ASIC templates	Best	Bad	Best	Bad	Bad
Enterprise-grade campus differentiation					
Line-rate encryption MACsec, WAN MACsec, NetFlow	Best	Partial	Partial	Bad	Partial
Unmatched flexibility Customizable ASIC templates, MPLS, GRE, NAT support	Best	Bad	Best	Bad	Bad
400G leadership in campus Support for 10G to 400G speeds	Best	Best	Bad	Bad	Bad

Legend

Best

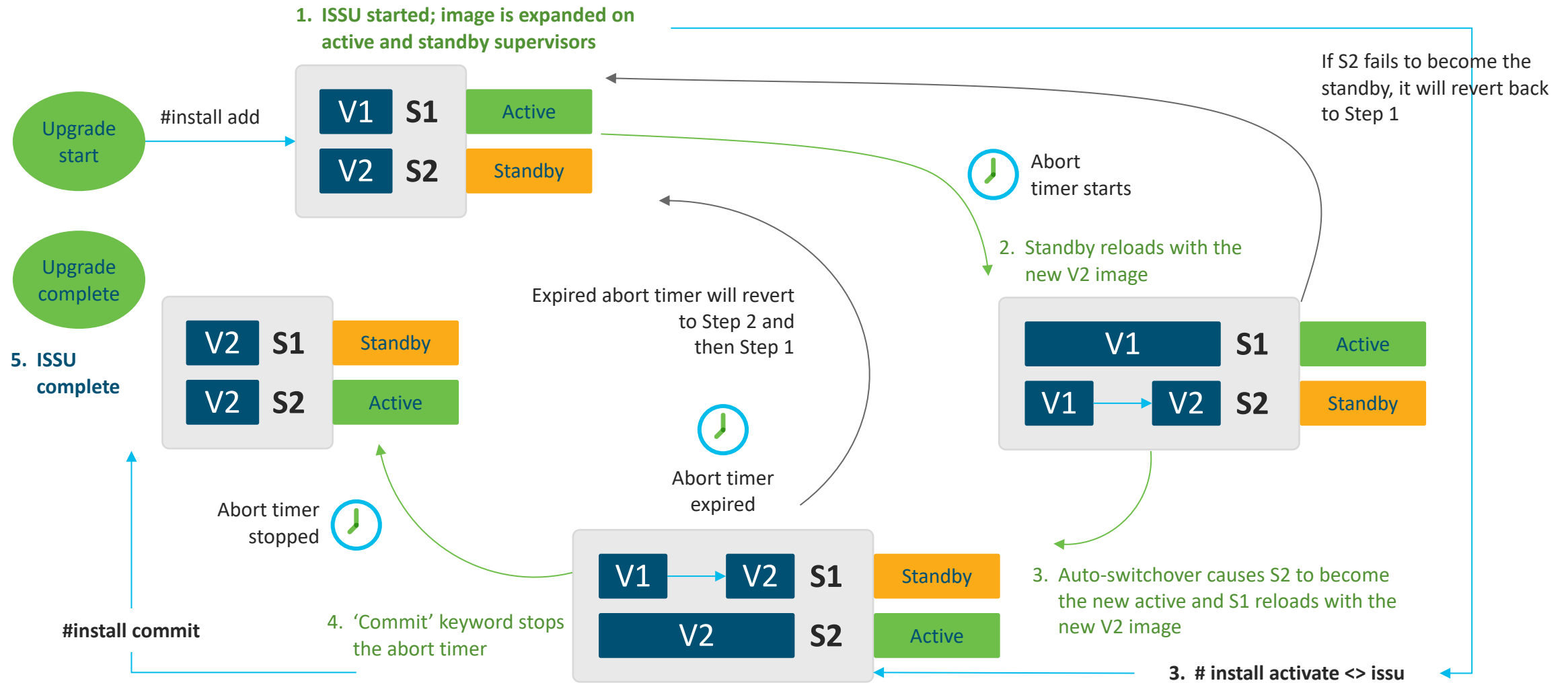
Partial

Bad

Highlight higher scale, performance, and 400G leadership in campus.
 Showcase unmatched customizable ASIC template capability.
 Win with Catalyst 9500X differentiation against the competition.

High Availability

Cisco Catalyst 9000 Series ISSU workflow*



*ISSU is applicable for SVL setups

ISSU Upgrade steps

Three-step process:

- Install add file <tftp/ftp/flash/disk:*.bin>
- Install activate ISSU
- Install commit

Granular control on the upgrade process with the ability to roll back

One-step process:

- Install add file <tftp/ftp/flash/disk:*.bin>activate
ISSU commit

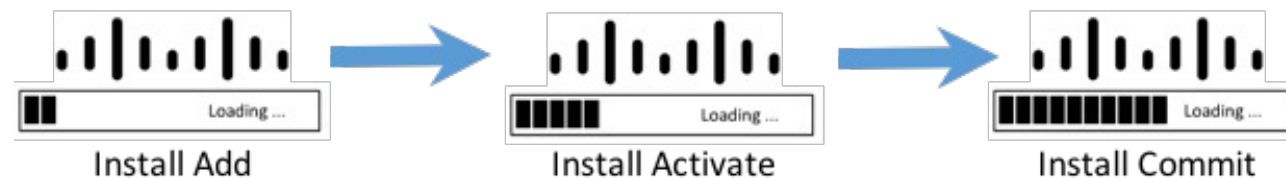
Single command to perform a complete ISSU

Software Maintenance Updates/ Patching

SMU is an emergency point fix positioned for expedited delivery to a customer in case of a network down or revenue affecting scenario.

Cold Patching: Install of a SMU will require a system reload in the first release. It is traffic impacting.

Hot Patching: Install of a SMU does not require a reload.



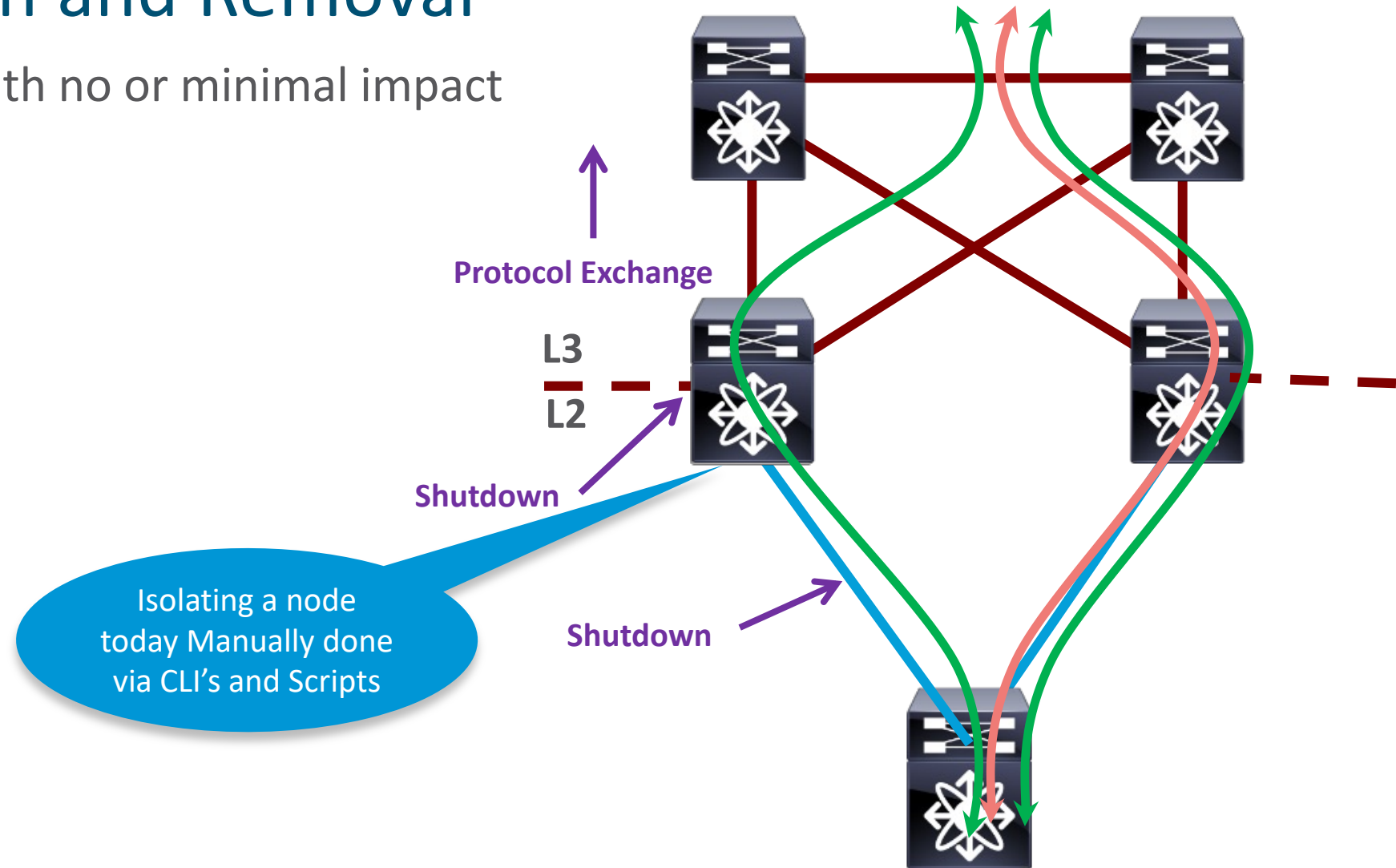
Graceful Insertion and Removal

Wish to Isolate a node with no or minimal impact

Hardware
Replacement

Software
Upgrades

Configuration
Changes



Graceful Insertion and Removal



Upgrades with no or Minimal Traffic Loss



Comprehensive Node Isolation Framework



Easy Execution with a single command



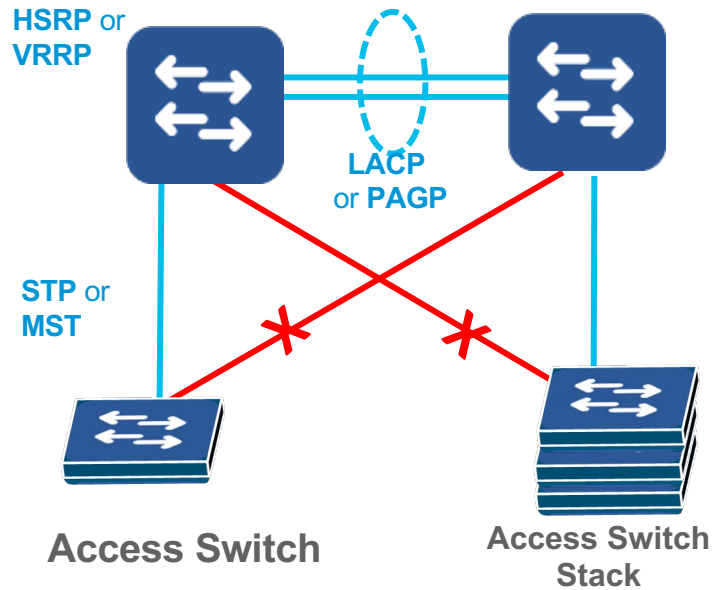
Highly Customizable workflow

**Simple
Customizable
Non-Traffic Impacting**

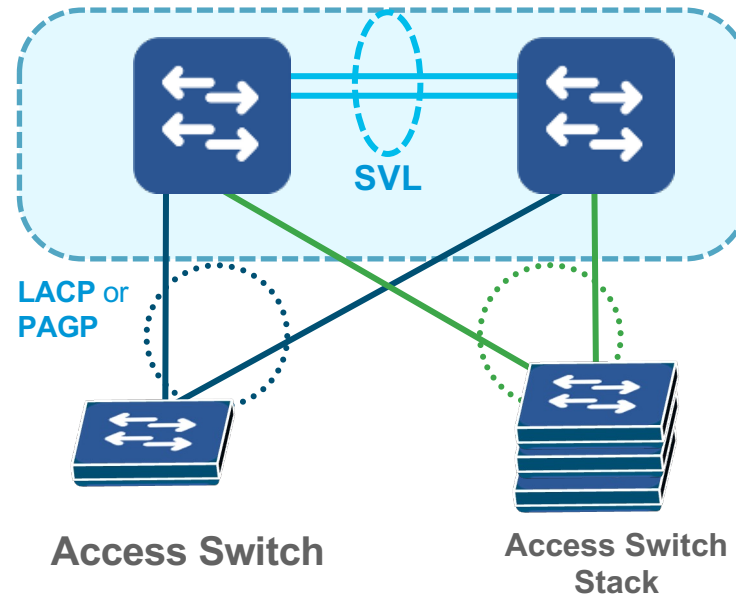
StackWise Virtual

Topology Comparisons

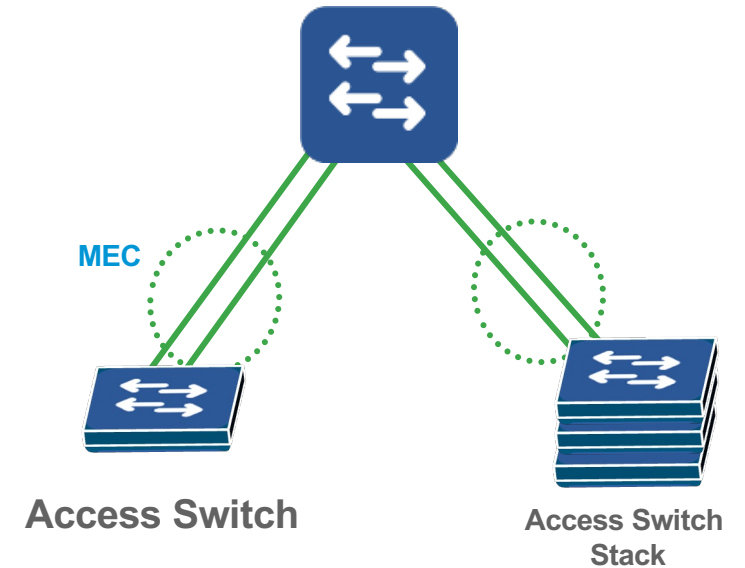
Traditional



SV - Physical



SV- Logical



Benefits of StackWise Virtual

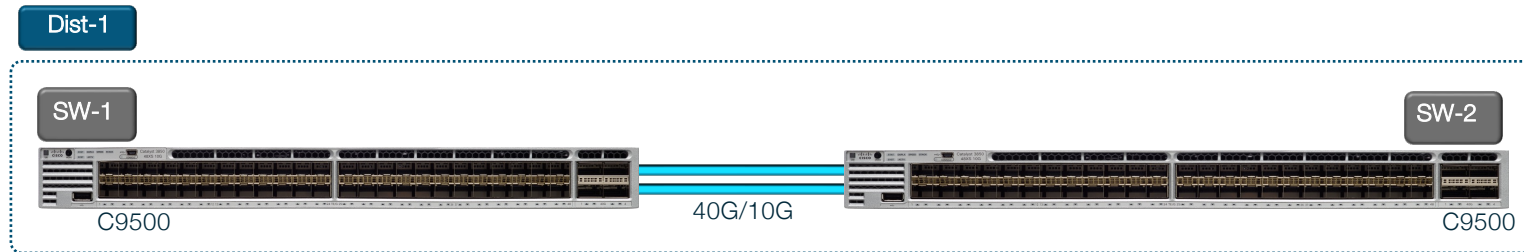
Simplify Operations by Eliminating STP, FHRP and Multiple Touch-Points

Double Bandwidth & Reduce Latency with Active-Active Multi-chassis EtherChannel (MEC)

Minimizes Convergence with Sub-second Stateful and Graceful Recovery (SSO/NSF)

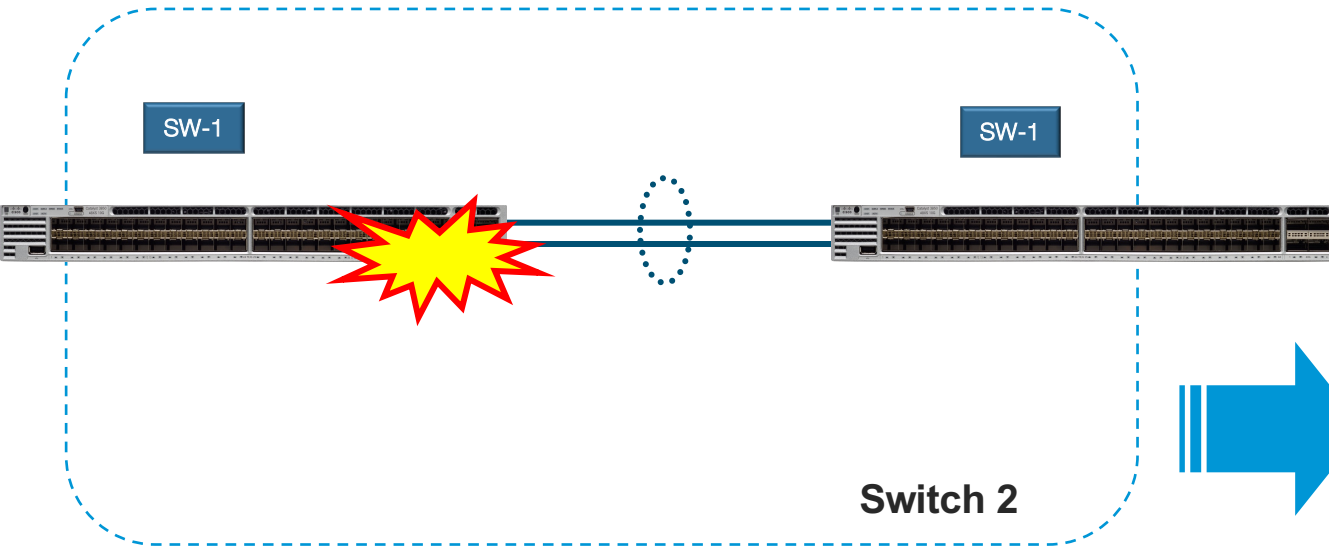
StackWise Virtual - 9500

Stacking and Cables



- Cisco StackWise Virtual is a Distribution layer technology allowing stacking of **only** 2 switches using any fixed front panel ports (*This may vary based on 9500 models – refer to limitations section*)
- Cisco Stackwise Virtual supports flexible distances with support of all supported cables and optics

StackWise Virtual Inter Chassis SSO/NSF



1

Virtual Switch incurs a failure of the (SSO) Active Switch 1

The Standby Switch detects failure by loss of all SVL ports, or no replies to SSO keep-alive packets

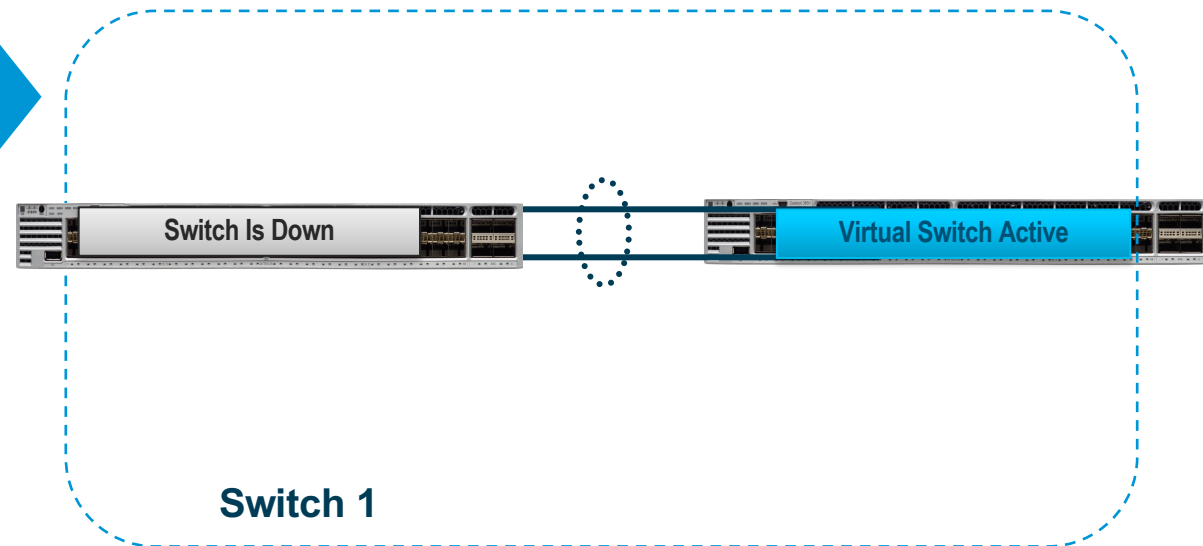
2

The original Standby Switch now takes over as the new Virtual Switch Active

Virtual Switch initiates Graceful Restart (NSF)

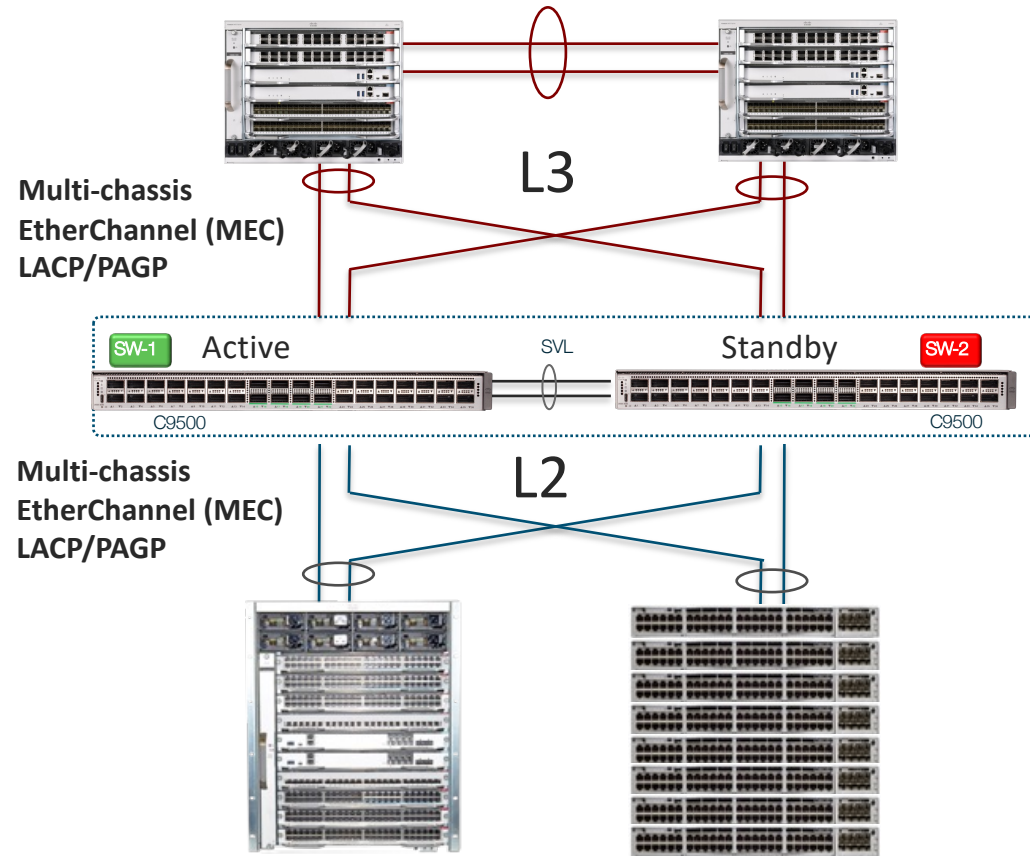
Non-Stop Forwarding of packets continues using hardware entries synched to Switch 2

NSF Aware neighbors exchange protocol updates with the new Virtual Switch Active



StackWise Virtual Platform Support

StackWise Virtual Design

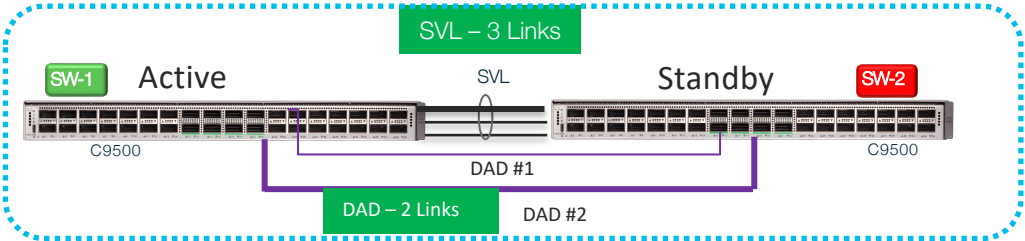
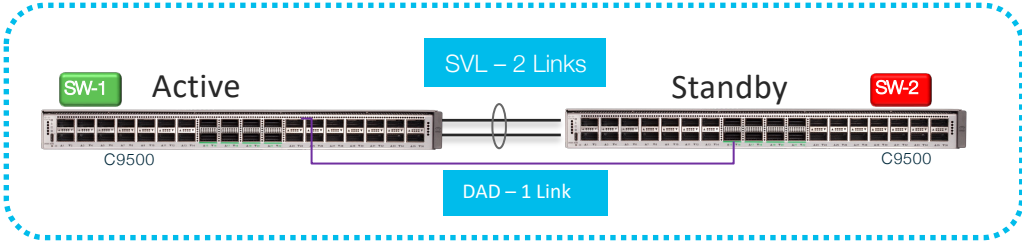


	SW-1 & SW-2	SW-1 & SW-2	SW-1 & SW-2	SW-1 & SW-2
Model	9400, 9500 & 9600	9400X	9500X-28C8D & 9600X	9500X-60L4D
Software Version	16.8.1/16.9.1*	17.9.1	17.10.1	17.11.1
Software License	Network Advantage	Network Advantage	Network Advantage	Network Advantage
Inter-Chassis Link	400, 200, 100, 40, 25 & 10G	100, 40, 25 & 10G	400, 100, 40 & 10G	400, 100, 40 & 10G
Max Inter-Chassis Link	8	8	8	8
Dual-Active Detection Link	4	4	4	4

- Sub-second traffic convergence with centralized control plane
- Traffic load-balancing with Active-Active Multi-chassis EtherChannel and distributed forwarding Architecture
- Only 1 supervisor per chassis participates in SVL except in quad-supervisor RPR

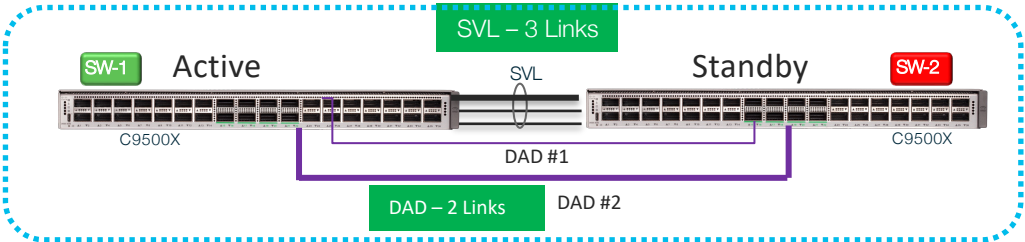
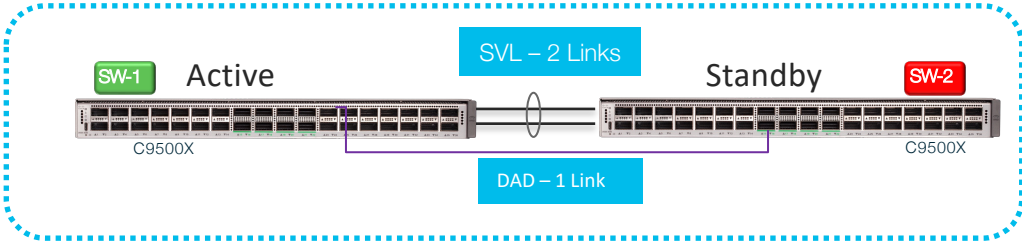
StackWise Virtual Enhancements for C9500X

Adding/Deleting Additional SVL or DAD Link – Requires a Reload of the entire SVL Pair



Adding/Deleting Additional SVL or DAD Link – Reload not required

IOS-XE 17.10.1+ **NEW**



Platform Support and Limitations

Platform / Model	SVL Ports	DAD Ports
9500-16X/40X	Any ports (downlink:10G; uplink:10G/40G) No breakout/QSA Support	Any ports (downlink:1G/10G; uplink:1G/10G/40G) No breakout/QSA Support
9500-12/24Q	Any ports (40G) No breakout/QSA Support	Any ports (40G) No breakout/QSA Support
C9500-24Y4C, C9500-48Y4C	Any port (downlink: 10G/25G; uplink: 10G*/40G/100G)	Any port (downlink: any speed; uplink:10G*/40G/100G)
C9500-32QC	Any port in default mode (10G*/40G/100G)	Any port in default mode (1G*/10G*/40G/100G)
C9500-32C	Port 1-16 (10G*/40G/100G) No breakout support	Port 1-16 (1G*/10G*/40G/100G) No breakout support
9500X-28C8D 17.10.1+	(10G*/40G/100G/400G)	(10G*/40G/100G/400G)
9500X-60L4D 17.11.1+	(10G*/40G/100G/400G)	(10G*/40G/100G/400G)

update

* With QSA adapter

Cisco Catalyst 9500 Series Security overview

Cisco Catalyst 9000 Platform Trustworthy Systems

Design/
Develop

Plan/
Order

Source

Make

Quality

Delivery

Service/End
of Life (EOL)

Physical security practices + security technology innovations + logical security processes

PnP SUDI support
Two-way trust

Secure boot
Boot sequence check

Image signing
Authentic OS

**Integrity
verification**
Malware protection

**Hardware
authenticity**
Genuine hardware

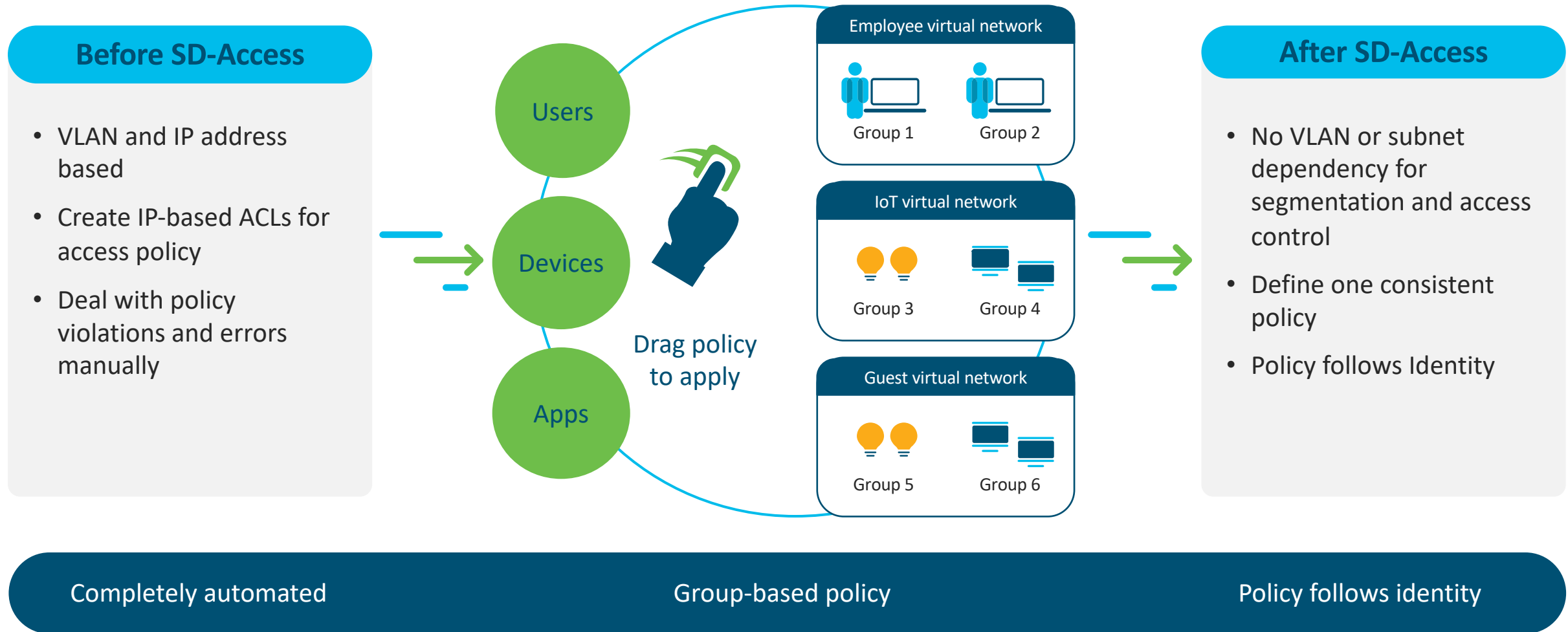
Runtime defenses
64-bit ASLR



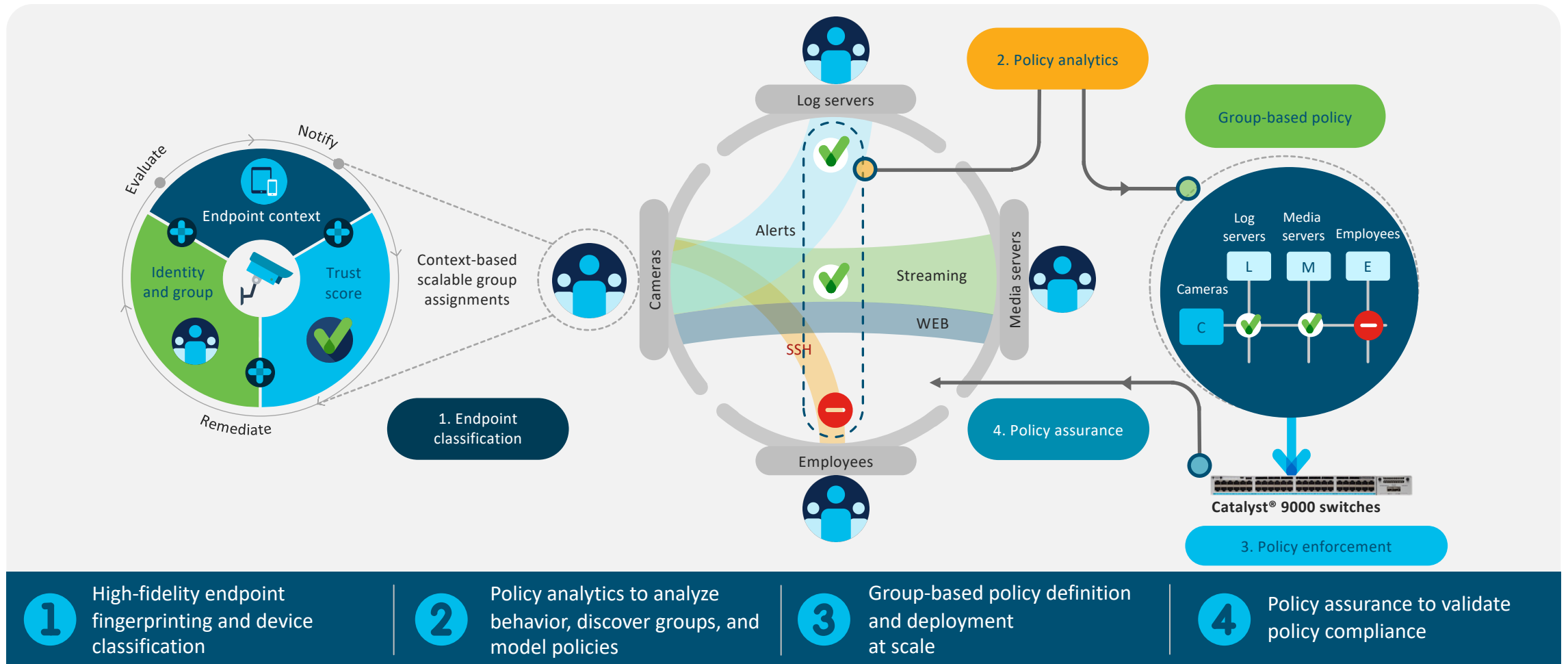
Cisco® trustworthy systems use industry best practices to help ensure full development lifecycle integrity and end-to-end security

Segmentation Agility with Security

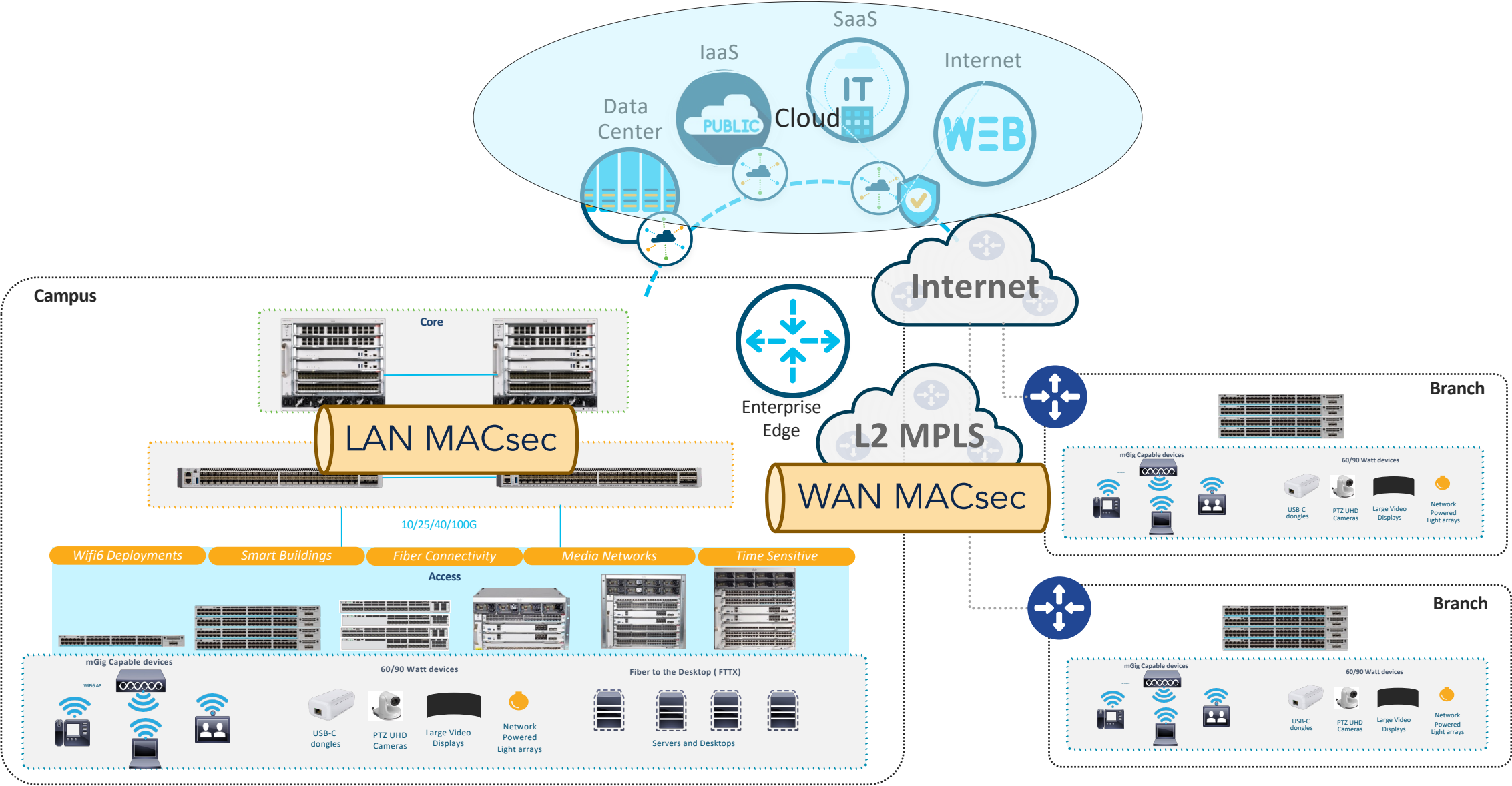
Secure onboarding of users and devices with flexible authentication and segmentation



SD-Access segmentation simplified through policy analytics

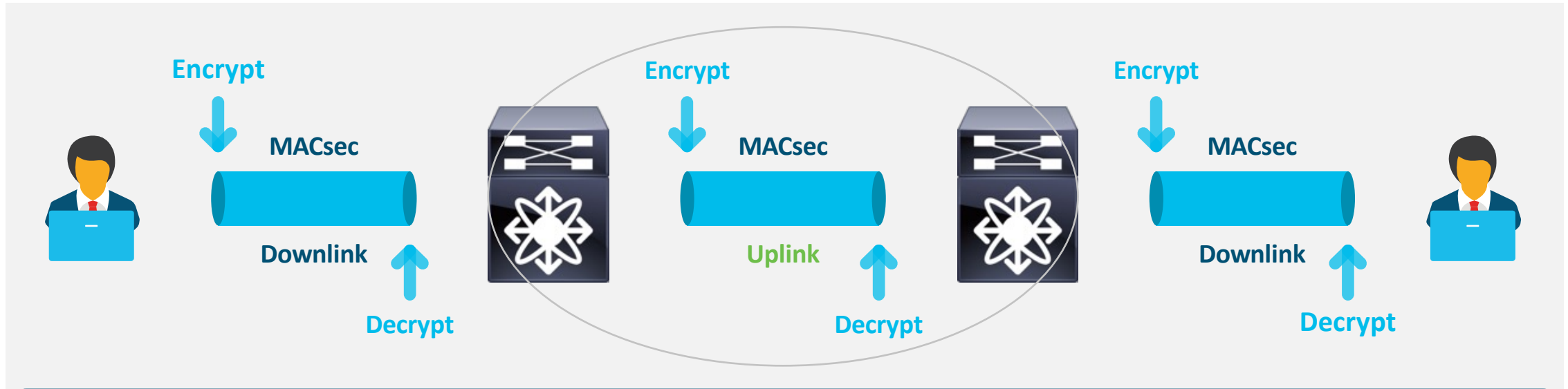


End-to-End Security for Campus



MACsec

Hop-by-hop encryption via 802.1AE

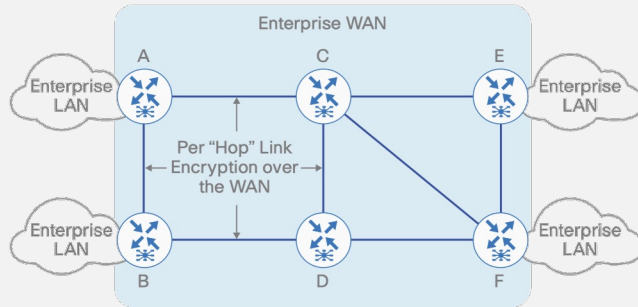


- Packets are encrypted on egress; decrypted on ingress
- Offers line-rate encryption on all ports and speeds (1G, 2.5G, 5G, 10G, 25G, 40G, and 100G)
- Transparent to all upper-layer protocols
- Supports switch-to-switch and switch-to-host MACsec
- 256-bit MACsec-capable between switch to switch
- Manual or 802.1X modes supported

WAN MACsec overview and use cases

Enabled in hardware on Catalyst 9000 Switches

MACsec

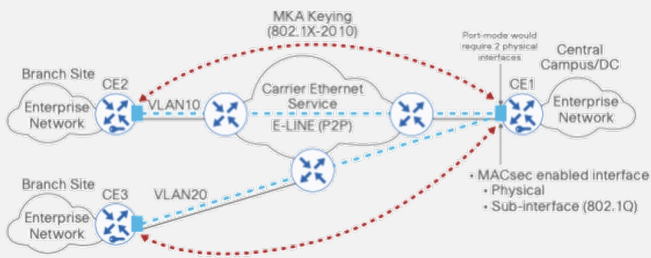


- Hop-by-hop encryption
- Directly connected Layer 2 links **only**
- Secure any direct link in campus/ WAN, including DWDM
- 256/128-bit AES encryption



Supported on **all Catalyst® 9000** models
All ports and speeds simultaneously

WAN MACsec



- End-to-end encryption across Layer 2 Ethernet WAN service
- EoMPLS/VPLS, Q-in-Q
- Point-to-point or point-to-multipoint
- Applications include secure site interconnect, DCI, storage replication
- 256/128-bit AES encryption



Catalyst 9600X



Catalyst 9500X

Supported on **Silicon One™** platforms*
All ports/speeds (up to 400G) simultaneously



Catalyst 9400X



Catalyst 9300X

Roadmap support access **Catalyst 9300X and 9400X**
Aggregate speed up to 100G

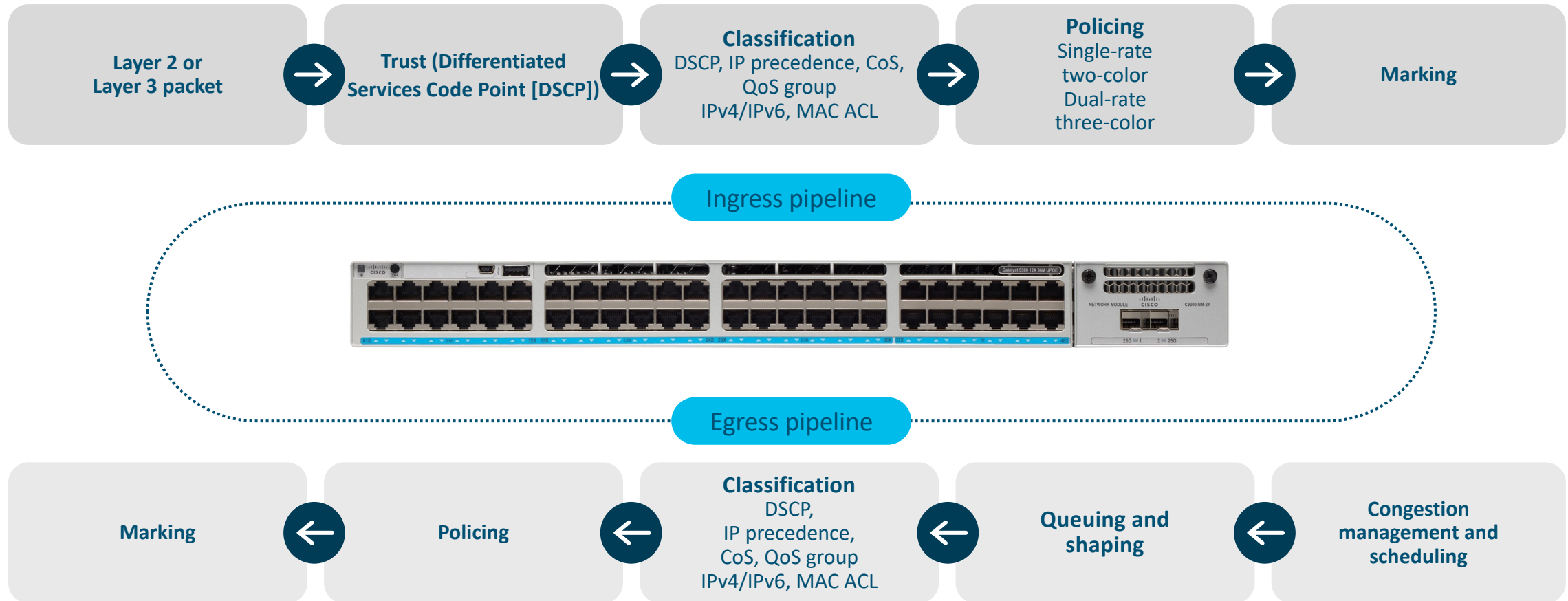
* Requires Release 17.8.1 and HSEC key (\$1 PID).

Quality of service

UADP 3.0 QoS

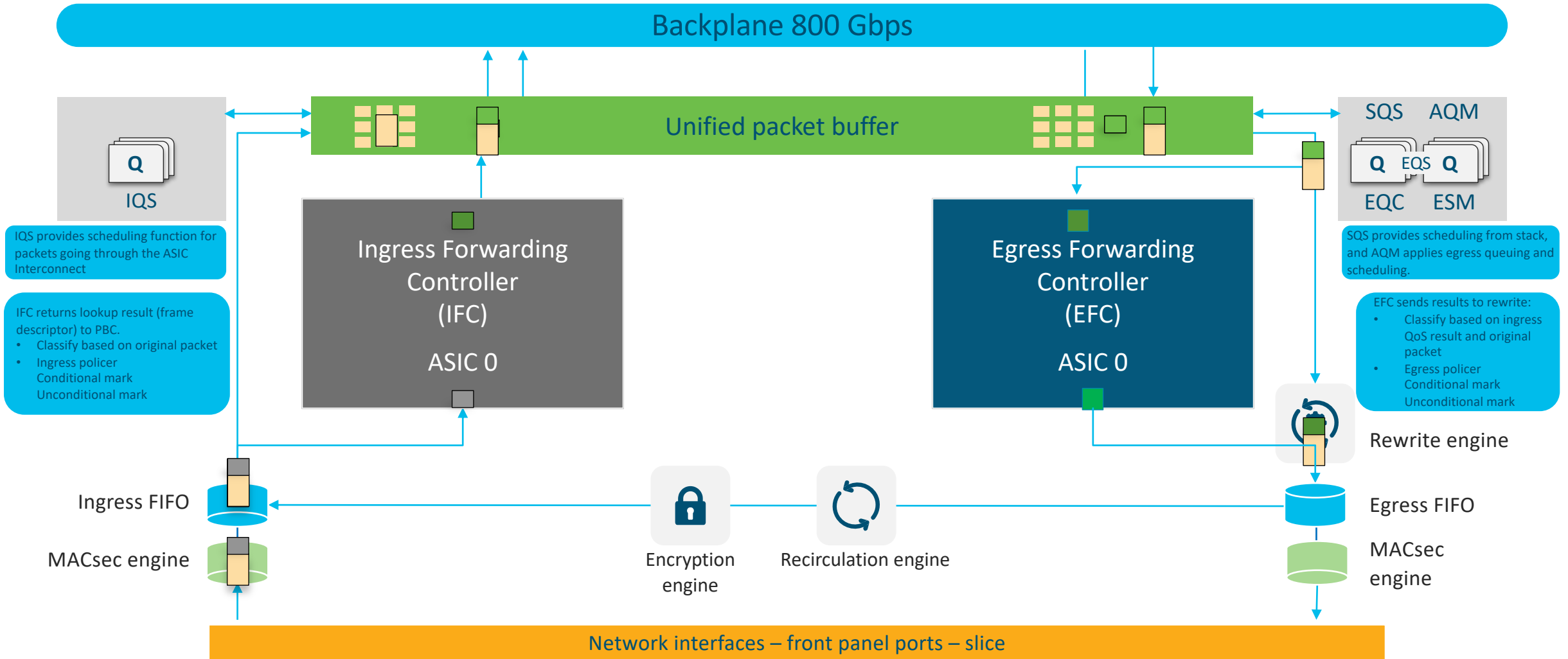
Cisco Catalyst 9500 Series – quality of service

- QoS is enabled by default
- All ports are trusted at Layer 2 and Layer 3 by default



Cisco Catalyst 9500 Series

QoS forwarding (ingress and egress)



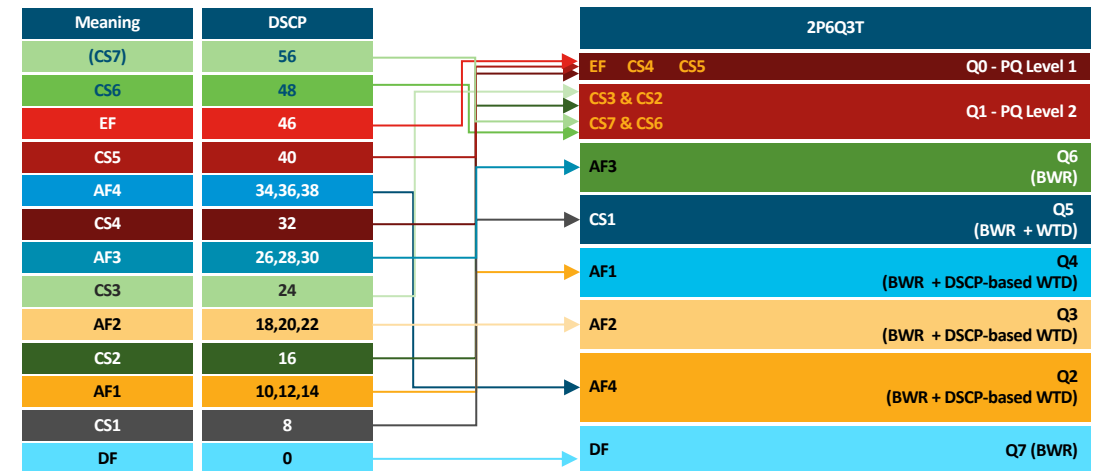
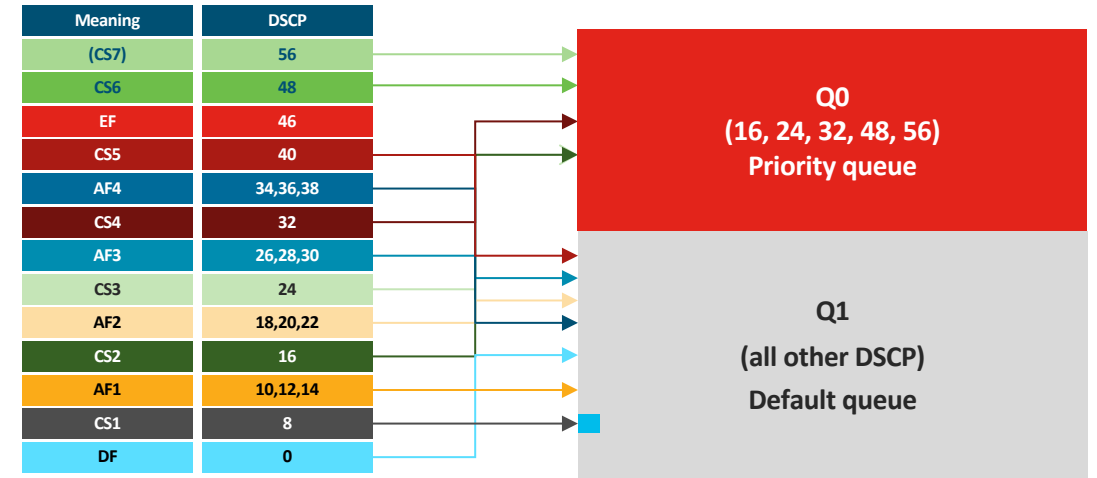
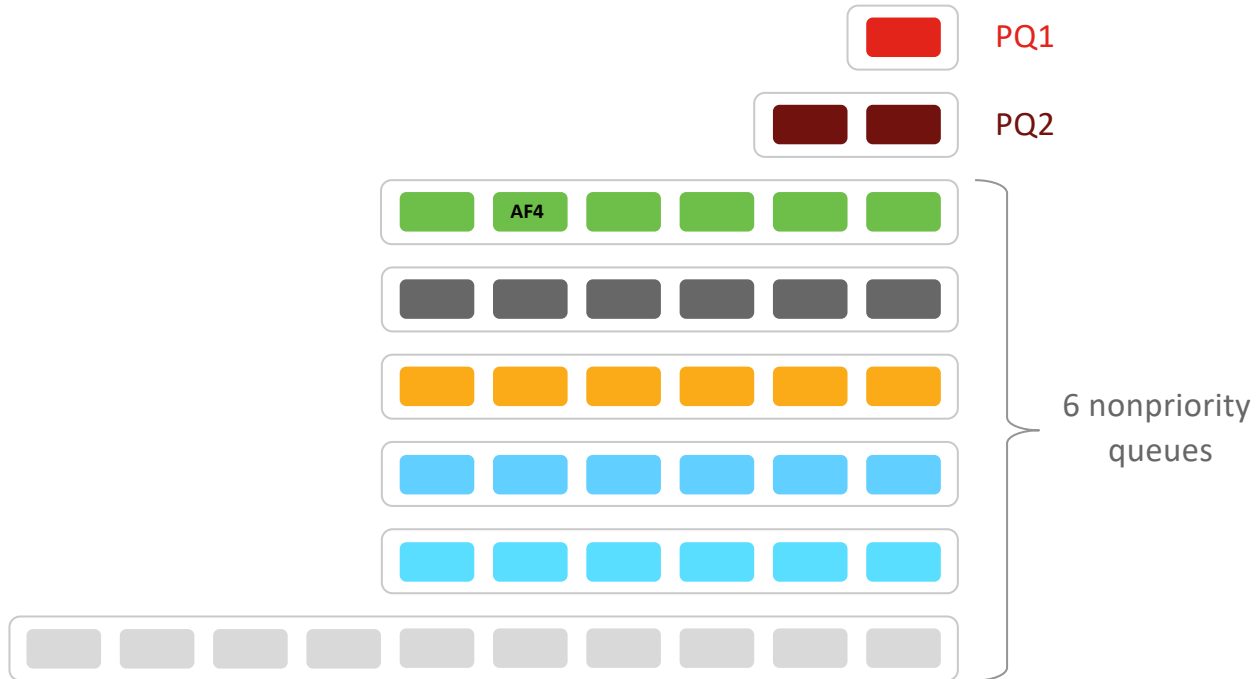
Cisco Catalyst 9500 Series

Hardware queues

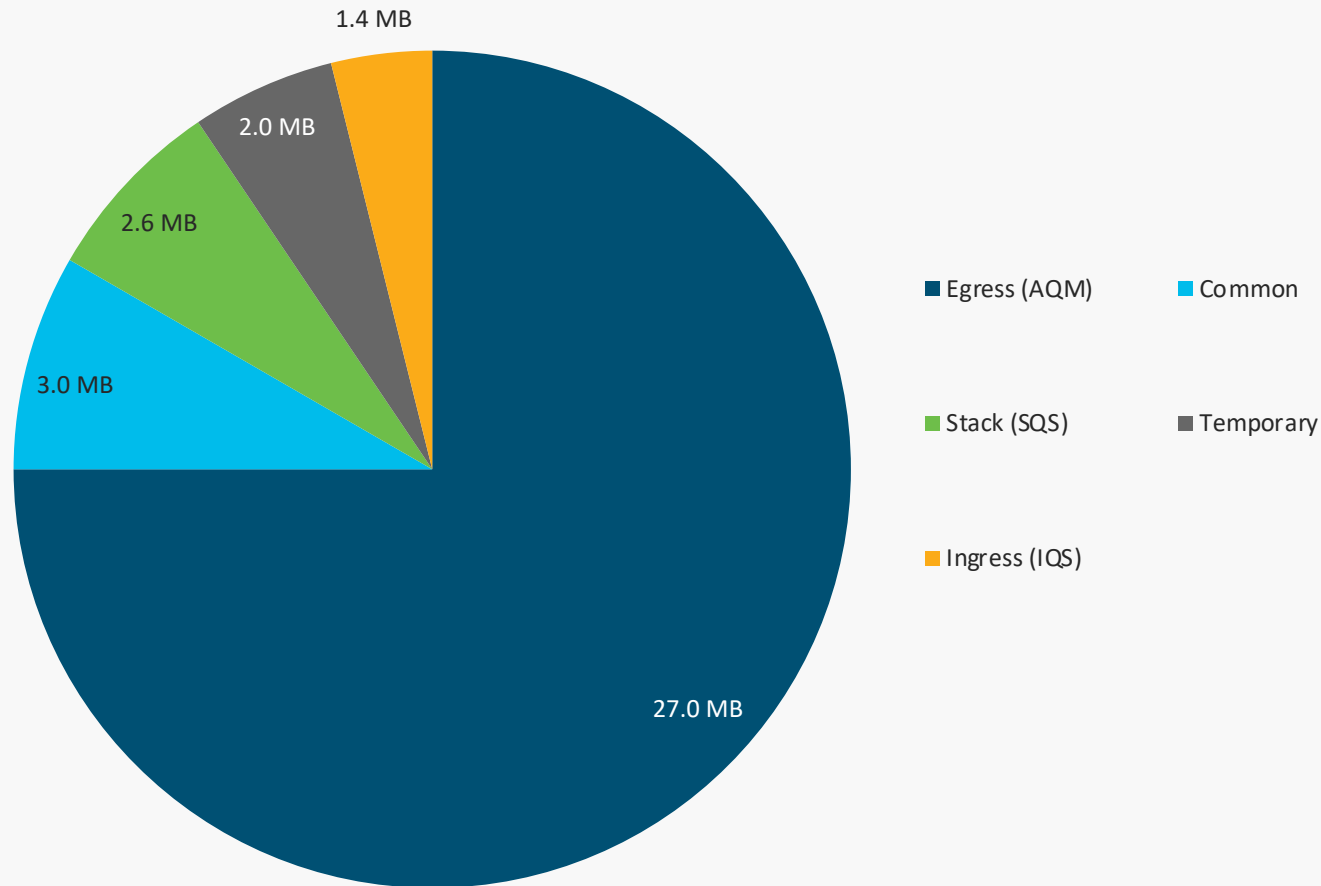
Default (2q3t)



Configurable (8Q3T/2P6Q3T)



Cisco Catalyst 9500 Series – unified packet buffer complex

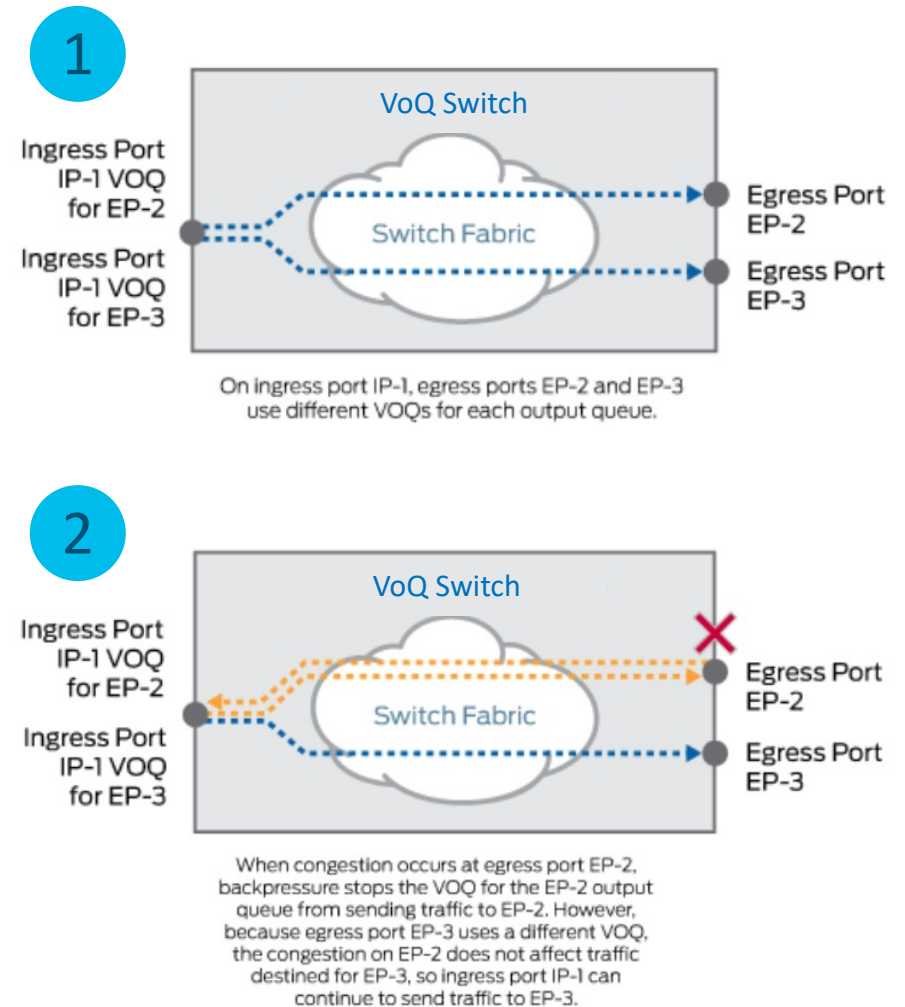
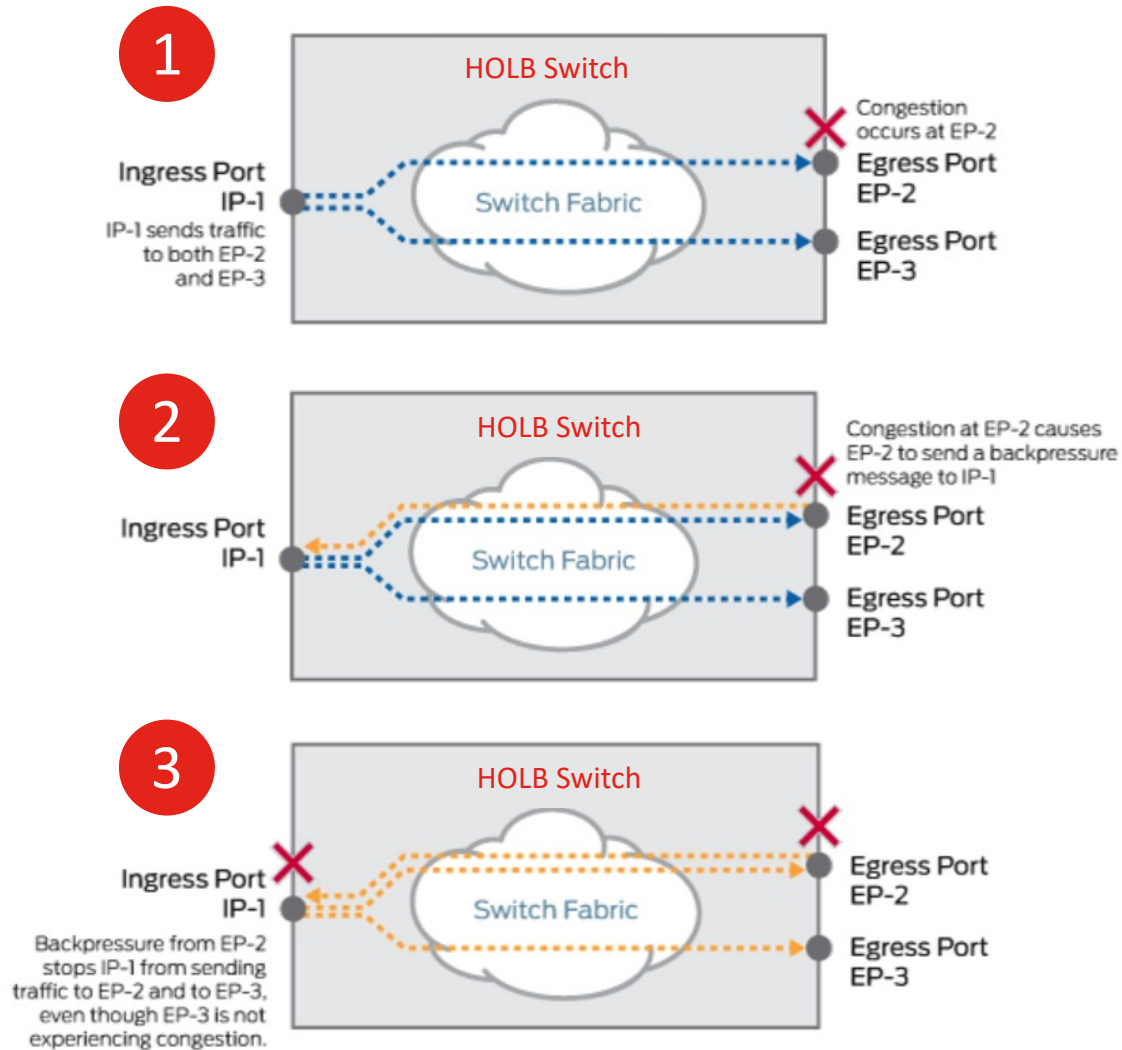


- 36-MB unified packet buffer is shared by ingress and egress data paths and between both cores
- Resources consuming packet buffer:
 - Ingress buffers (IQS)
 - Egress stack buffers (SQS)
 - Egress port buffers (AQM)
 - Temporary buffers
 - Common buffers

Silicon One QoS

VoQ Architecture and Head of Line Blocking

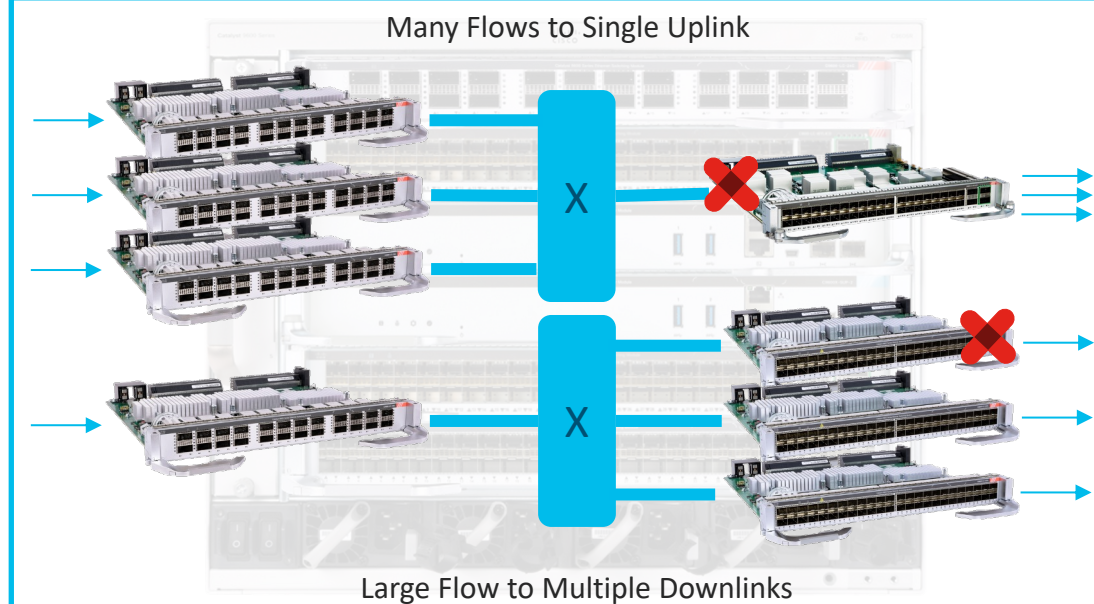
Virtual Output Queueing – Egress Optimized



Cisco 9500X – Why VoQ QoS?



No Head-of-Line Blocking



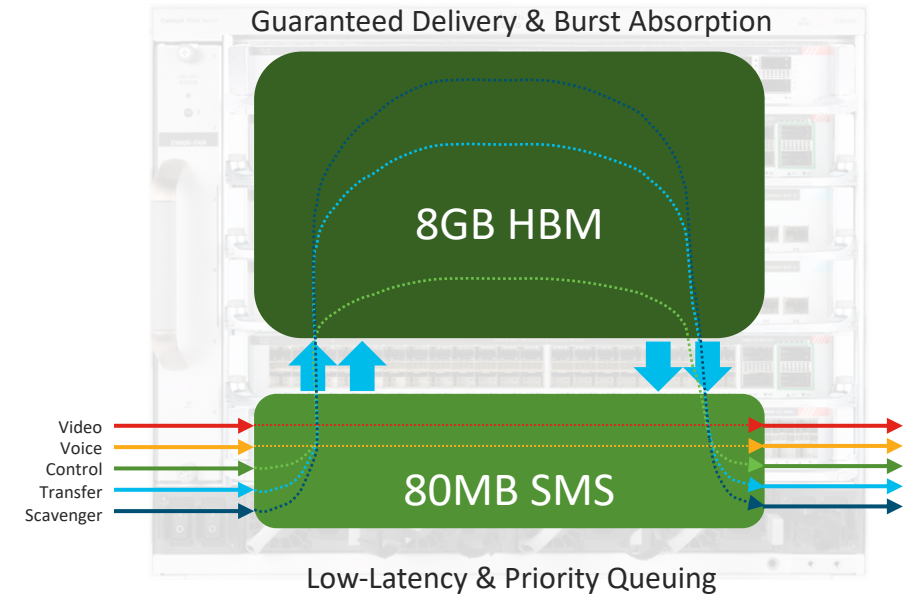
Many Flows to a Single Uplink

- Common on (expensive) WAN/Edge uplinks
- Even if bandwidth available, buffers can fill up

Large Flow to Multiple Downlinks

- Common for Multicast & Broadcast traffic
- One slow receiver can penalize other ports

Local vs. HBM Buffers



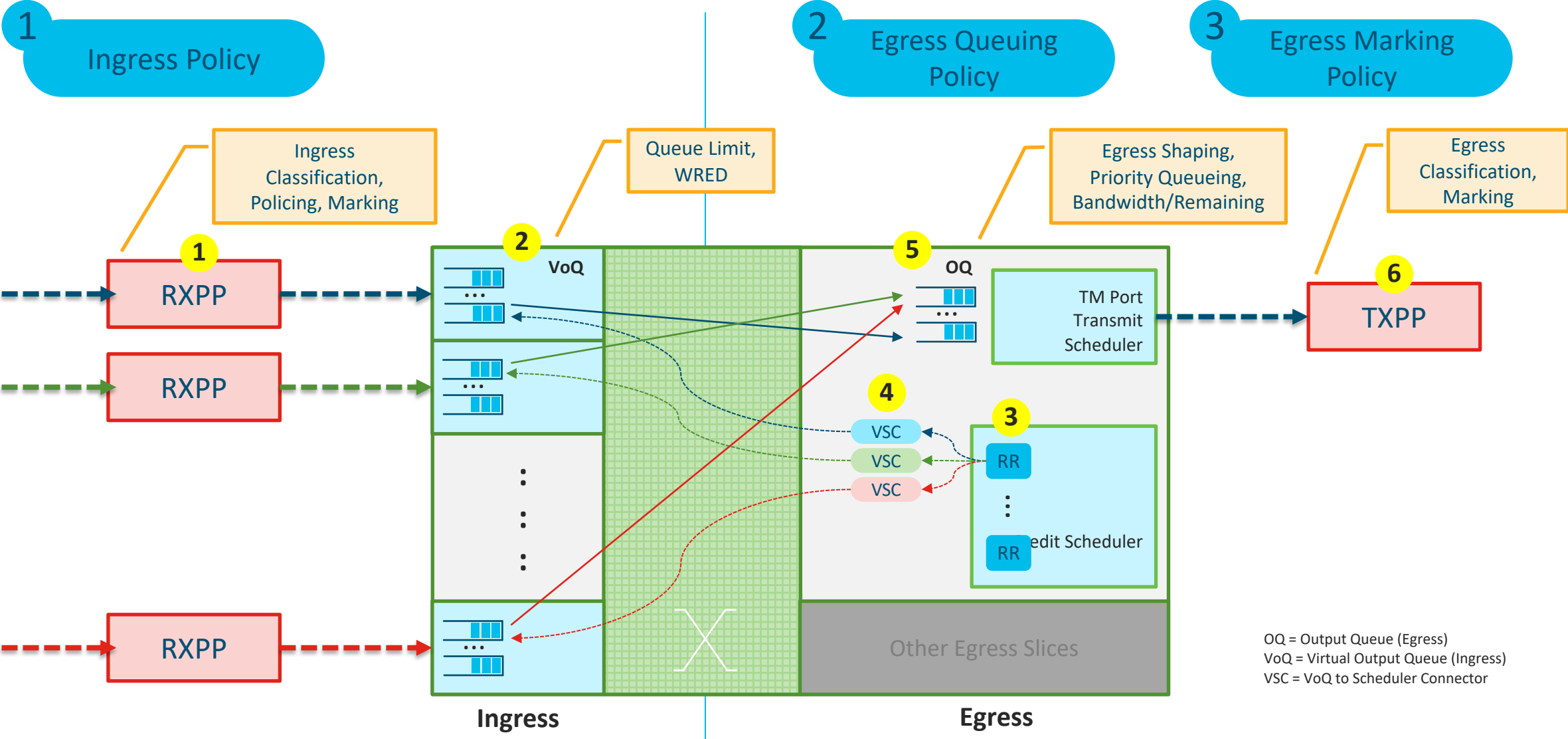
Low-Latency Local Shared Memory Buffers

- Voice & Video are very latency-sensitive
- Multiple levels of Strict Priority Queuing

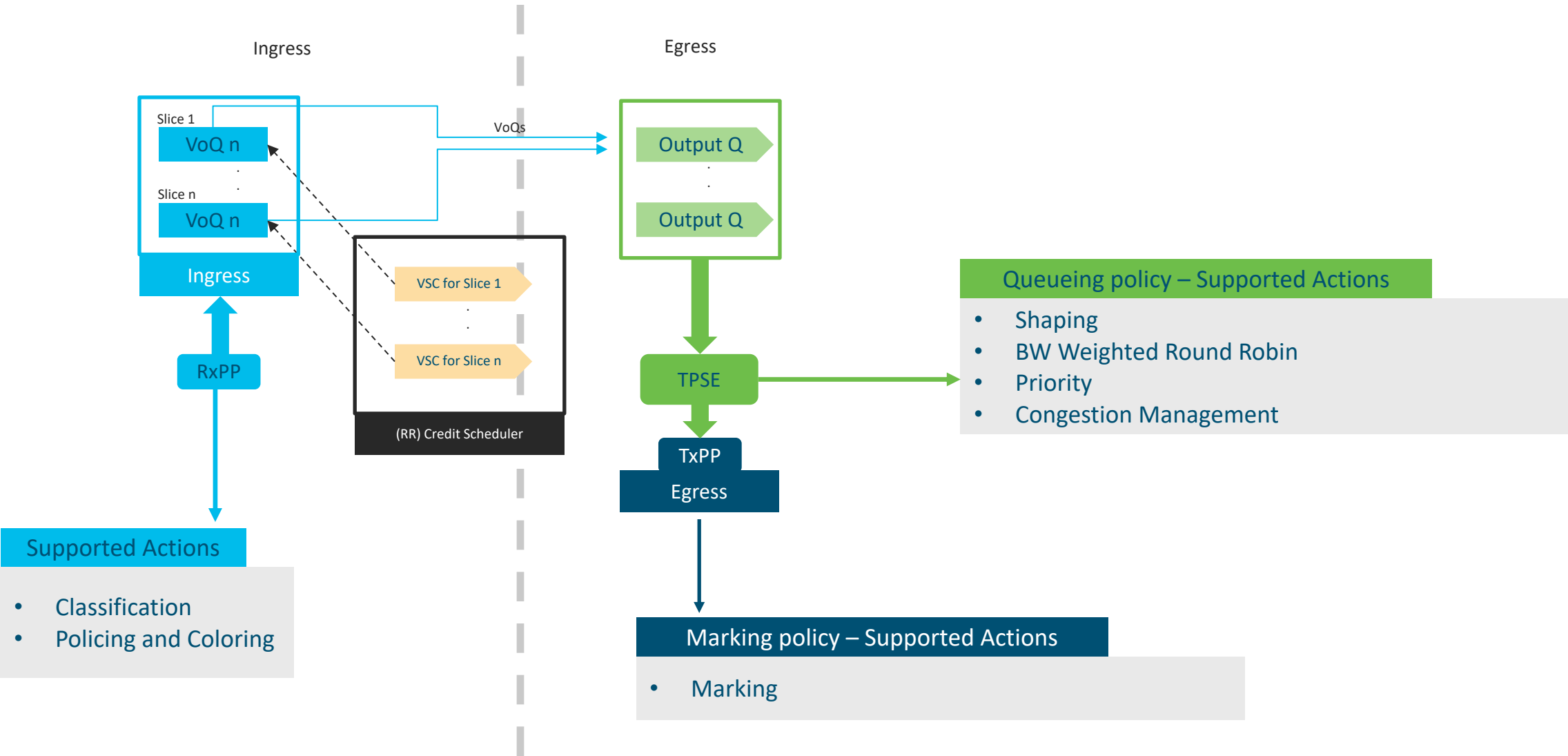
Deep High-Bandwidth Memory Buffers

- Guarantee delivery of session-oriented flows
- Reserve buffers to absorb occasional bursts

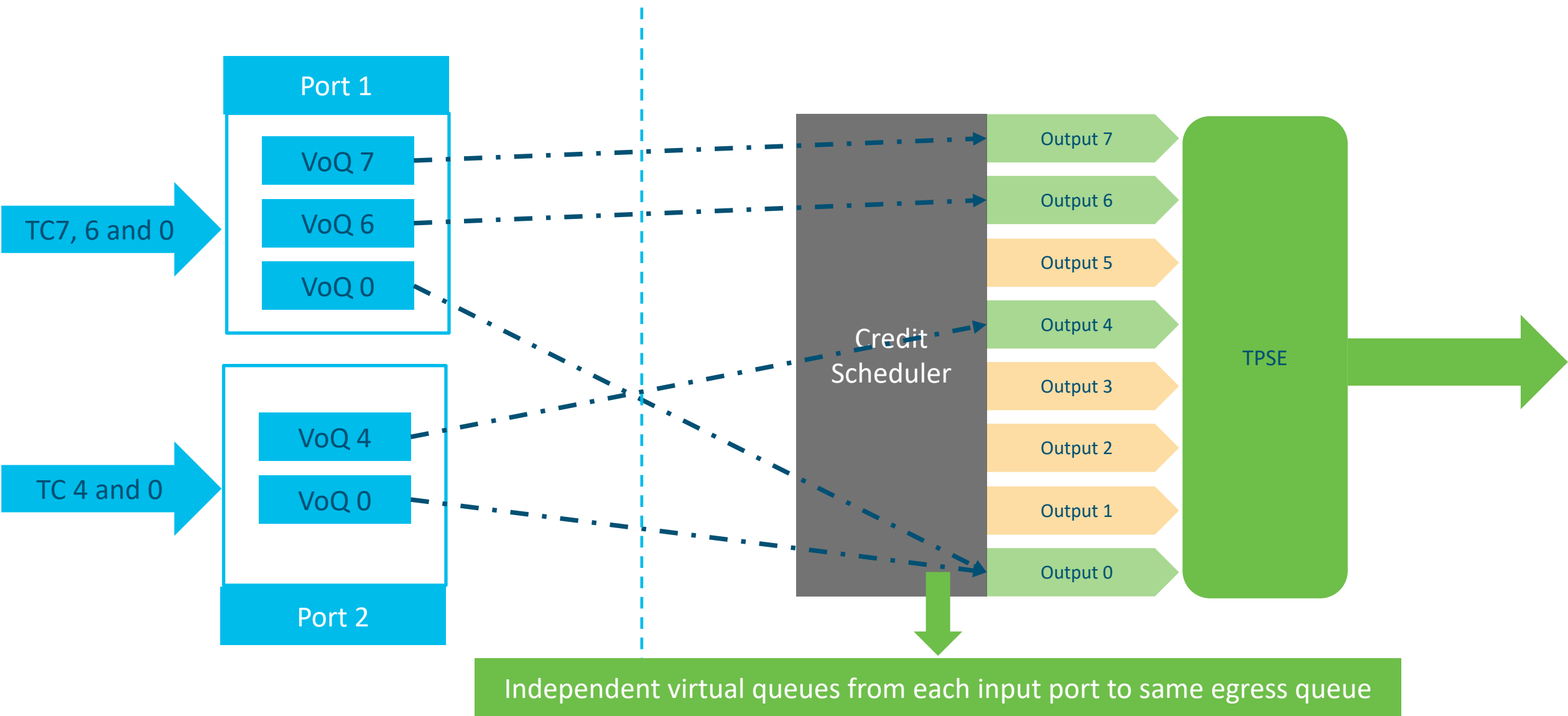
S1 Q200 – QoS overview



QoS Toolset



VoQ Mapping



Access control lists

Cisco Catalyst 9500 Series access control lists

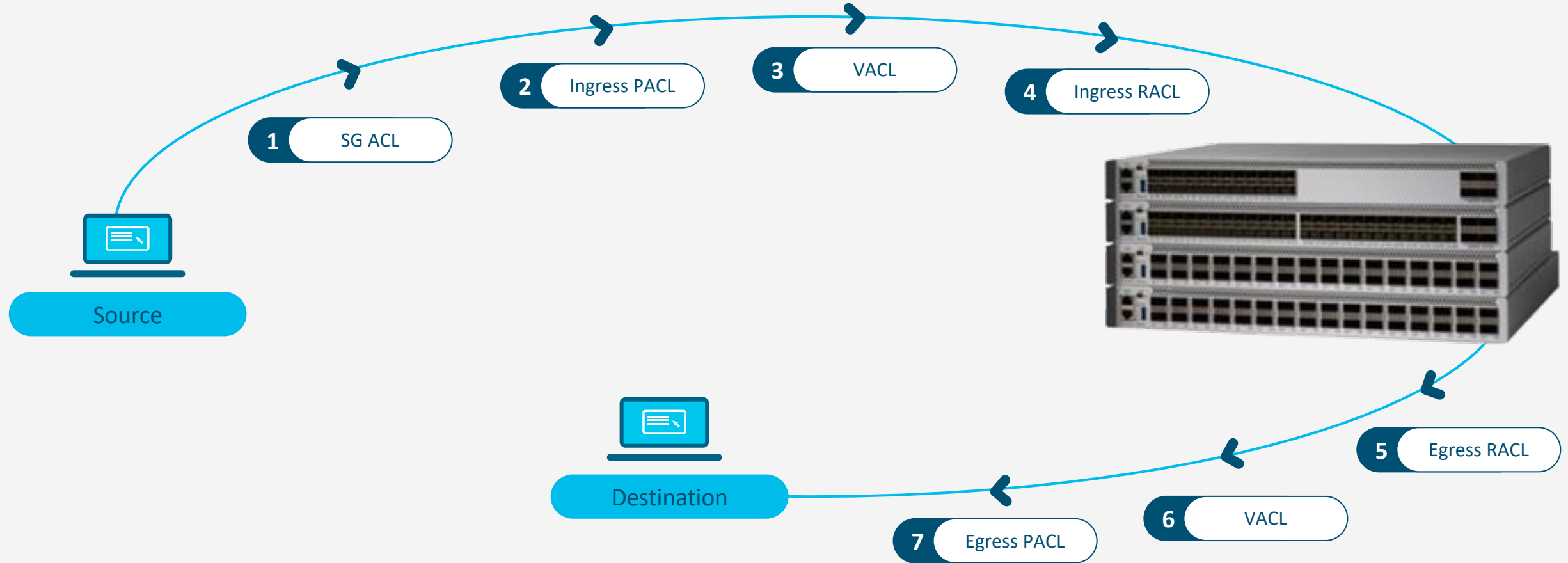
Four forms of security ACLs

The Cisco Catalyst 9500 Series supports four forms of security ACL: SG ACL, RACL, VACL, and PACL

Router ACL (RACL)	VLAN ACL (VACL)	Port ACL (PACL)	Security group ACL (SG ACL)
Used to permit or deny the movement of traffic between Layer 3 subnets	Used to permit or deny the movement of traffic between Layer 3 subnets and VLANs or within a VLAN	Used to permit or deny the movement of traffic between Layer 3 subnets and VLANs or within a VLAN	Used to permit or deny the movement of traffic based on the SGTs that are assigned
Applied as an input or output policy to a Layer 3 interface, Switch Virtual Interface (SVI), or Layer 3 EtherChannel interface	Applied as a policy to a VLAN; is inherently applied to both inbound and outbound traffic	Applied as a policy to a Layer 2 switch port interface or EtherChannel interface ; is applied to inbound traffic only	Applied as a policy to a Layer 2 switch port interface; is applied to inbound traffic only
Standard/extended ACLs	Standard/extended ACLs	Standard/extended/MAC ACLs	Standard/extended/MAC ACLs

Cisco Catalyst 9500 Series access control lists

Order of processing



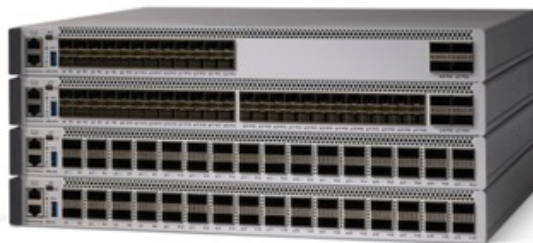
Cisco Catalyst 9500 Series - Access control lists

Hardware support

Create an ACL or classification policy, using the CLI or Network Management System (NMS)

```
ip access-list extended Internet
permit ip any host 10.2.2.4
permit ip any host 10.5.2.33
permit ip any host 10.11.0.0
permit ip any host 10.4.0.0
```

1



No hardware resources
Drop packet*

2

Full hardware support

- Router ACLs
- VLAN ACLs
- Port-based ACLs
- Role-based ACLs

3

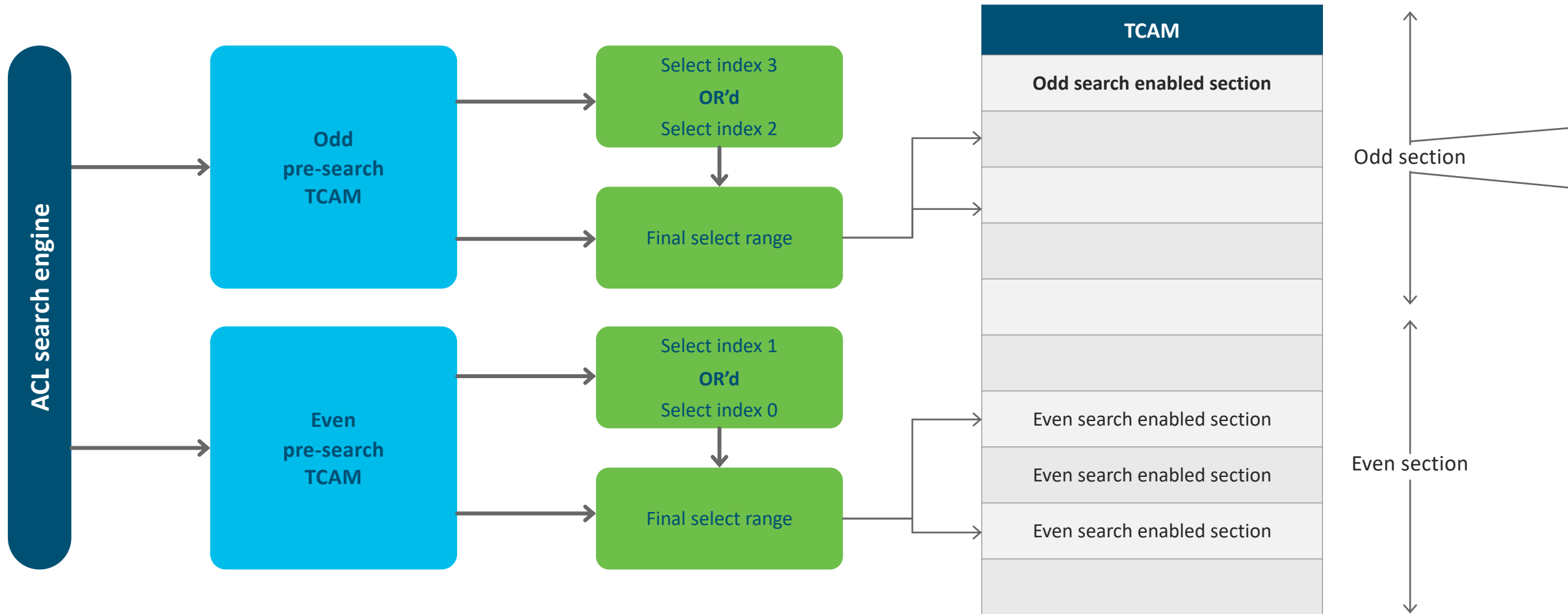
Hardware-assisted ACL features

- NetFlow
- NAT and PAT
- PBR
- WCCP
- Cisco TrustSec®

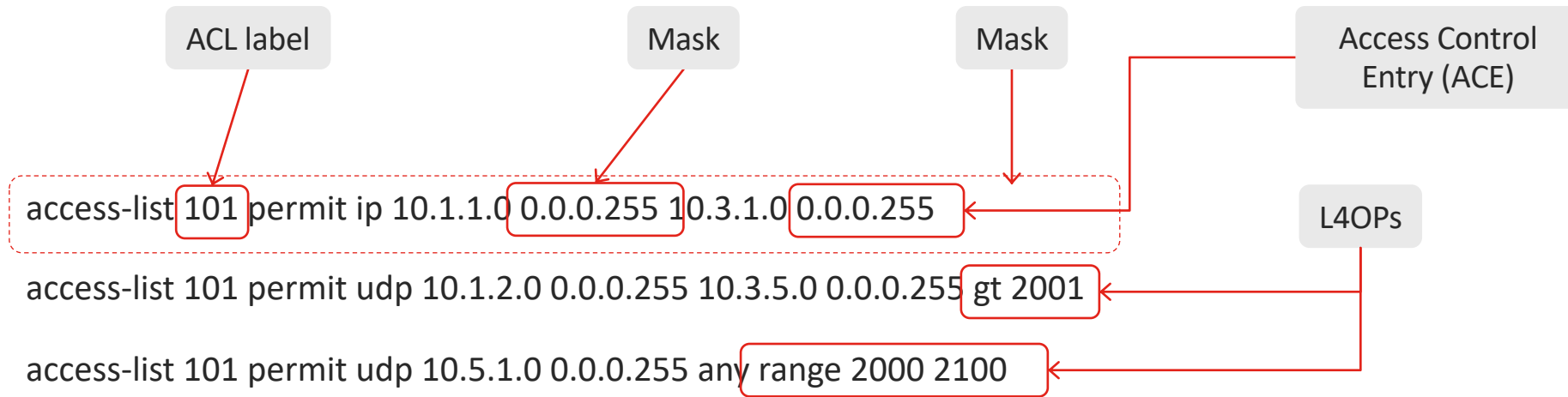
4

* Packets must be forwarded by software for any reason (for example, not enough hardware resources).
The switch forwards the packets only after applying ACLs on the packets.

Cisco Catalyst 9500 Series security TCAM lookup



Access control list terminology



What is an L4OP?

GT
(greater than)

LT
(less than)

NE
(not equal to)

RANGE
(from - to)

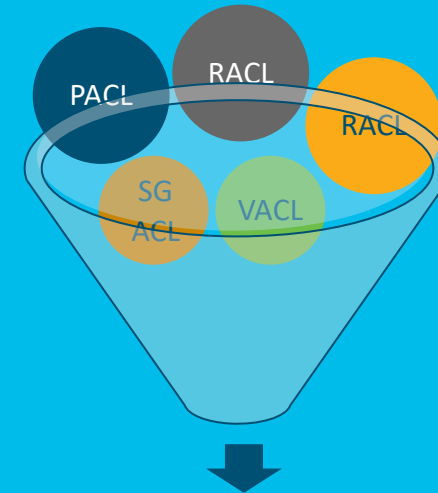
What is **NOT** an L4OP?

EQ
(equal to)

Cisco Catalyst 9500 Series – Hitless TCAM update

Starting
16.8.1

- **Allows updates to an ACL without interrupting traffic**
- Multiple features updated at once
 - IPv4, IPv6, MAC
 - PACL, RACL, VACL, and SG ACL
- Hitless update is enabled by default; can't be disabled
- Hitless update feature requires free ACL TCAM space for reprogramming but does consume any additional TCAM resources
- If not enough space in TCAM, falls back to old ACL method

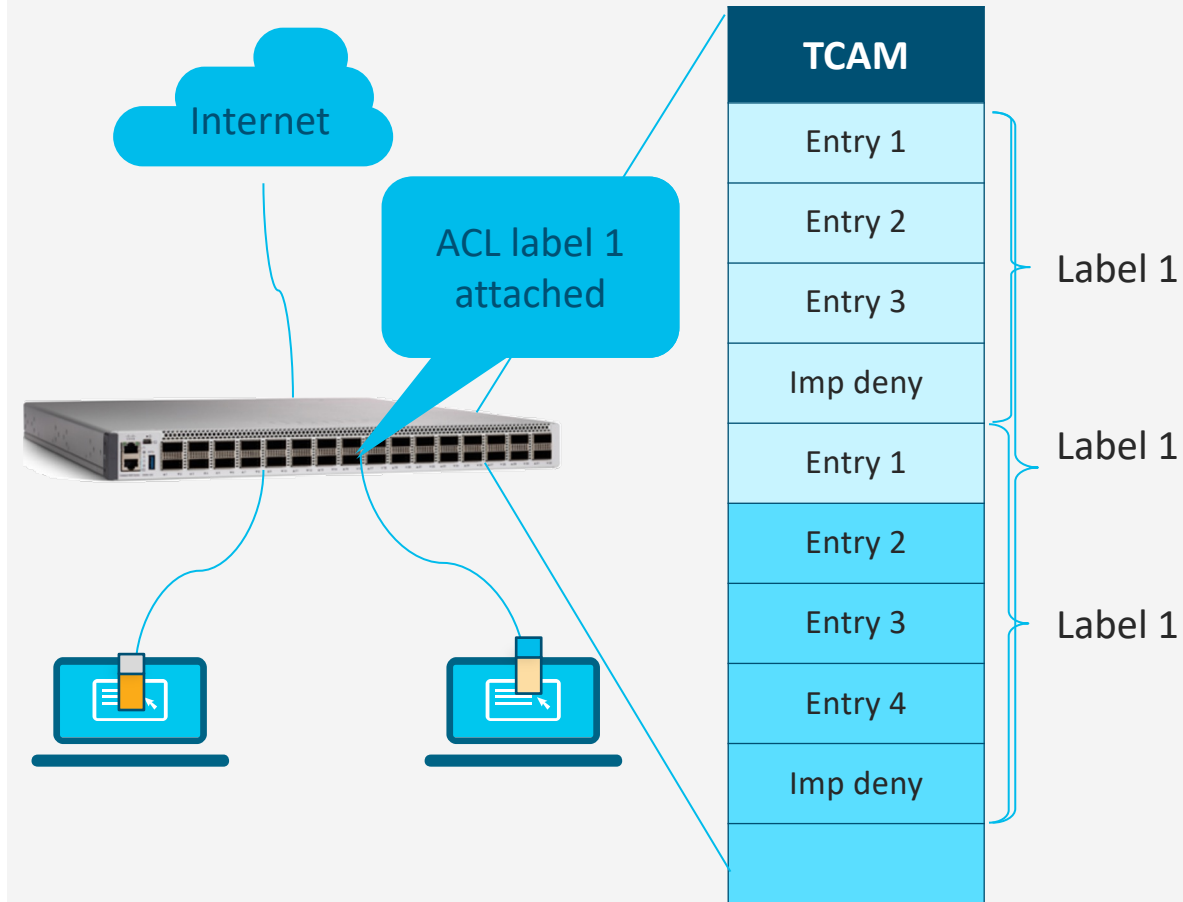


ACL updates

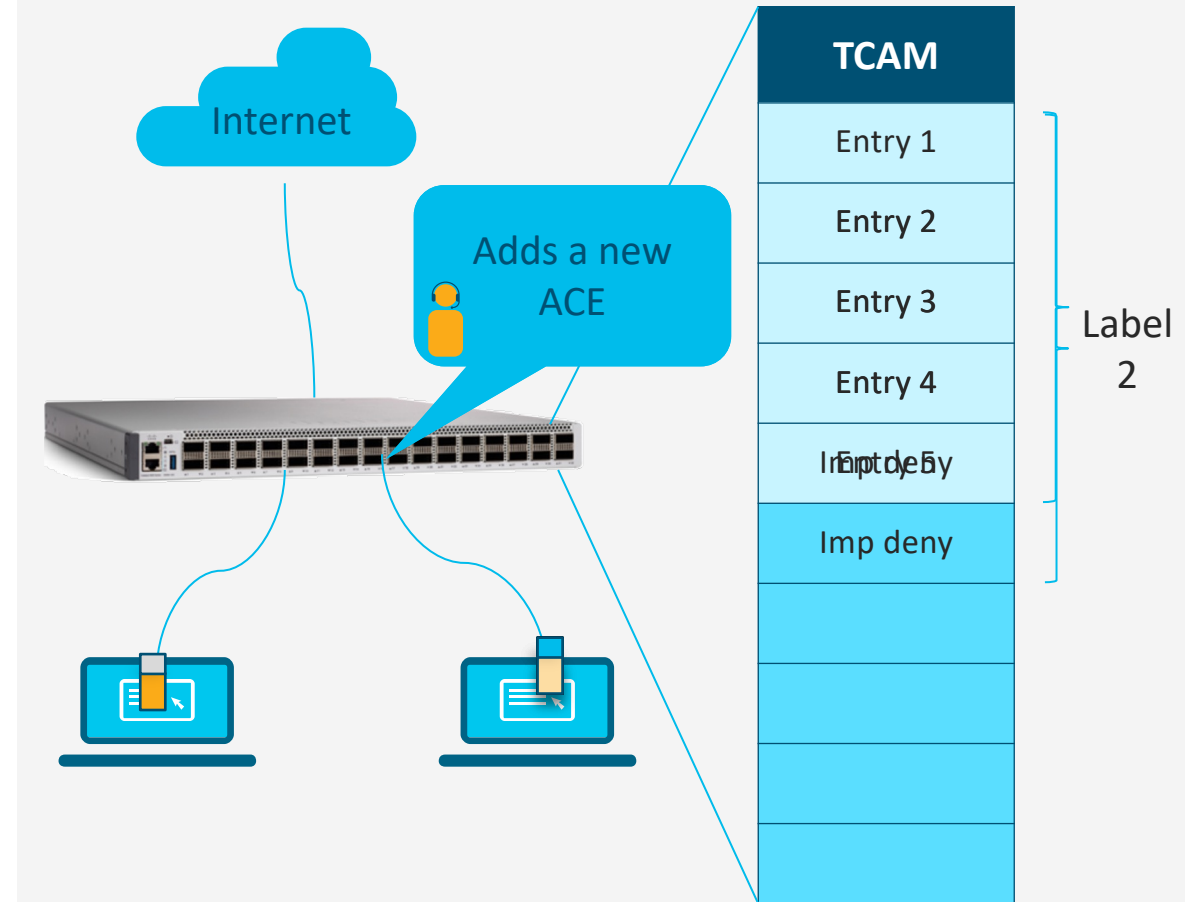


Cisco Catalyst 9500 Series– Hitless TCAM update

Example 1



Example 2





S1 Q200 - Central Database (CDB)

Onboard LPM, CEM & ACL memory

- CDB includes the **Central L2/L3 Forwarding** and **ACL** databases:

- **LPM** – IP/mask routing database implemented by **Longest Prefix Match** algorithm (extensible to HBM, for scale)

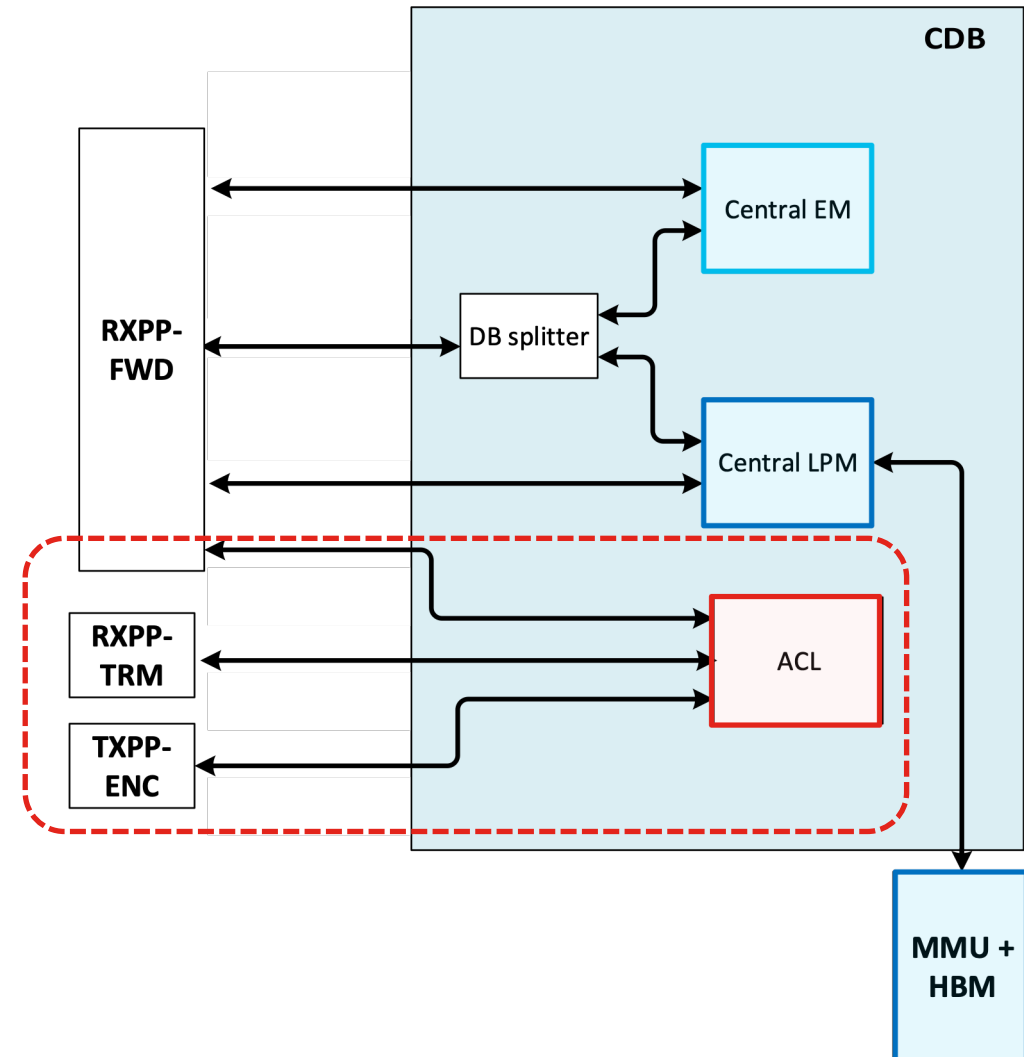
- **CEM** – MAC & IP Host (/48 or /32 - /128), Multicast and Label database implemented by an **Exact Match** algorithm

- **ACL** – **Access Control List** database, contains service Access Control Entries in TCAM

- **LPM & CEM** are accessed by **RX Forwarding** stage via 1 of 3 interfaces:

- **LPM** direct interface, or **CEM** direct interface
- **Splitter** – if accessing both, splitter merges response

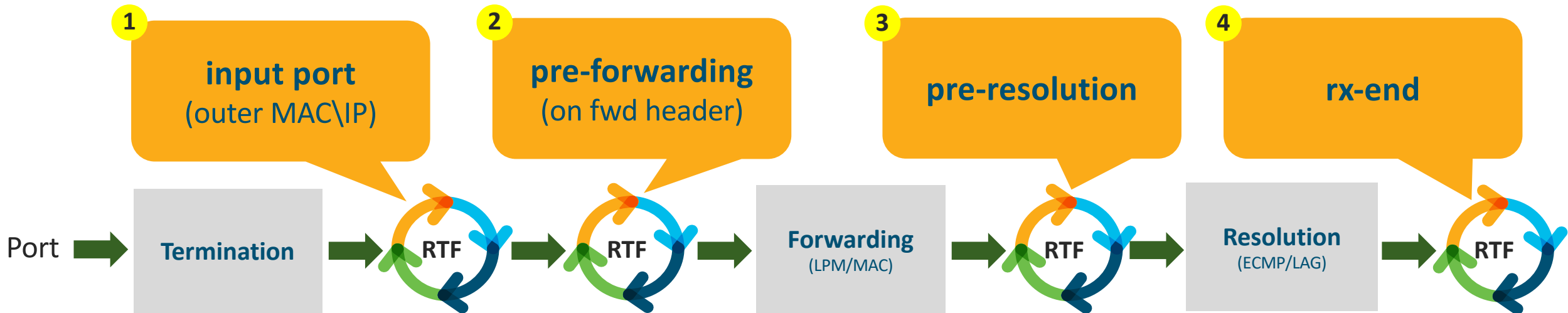
- **ACL** is accessed by **RX Termination**, **RX Forwarding** and **TX Encapsulation** stages





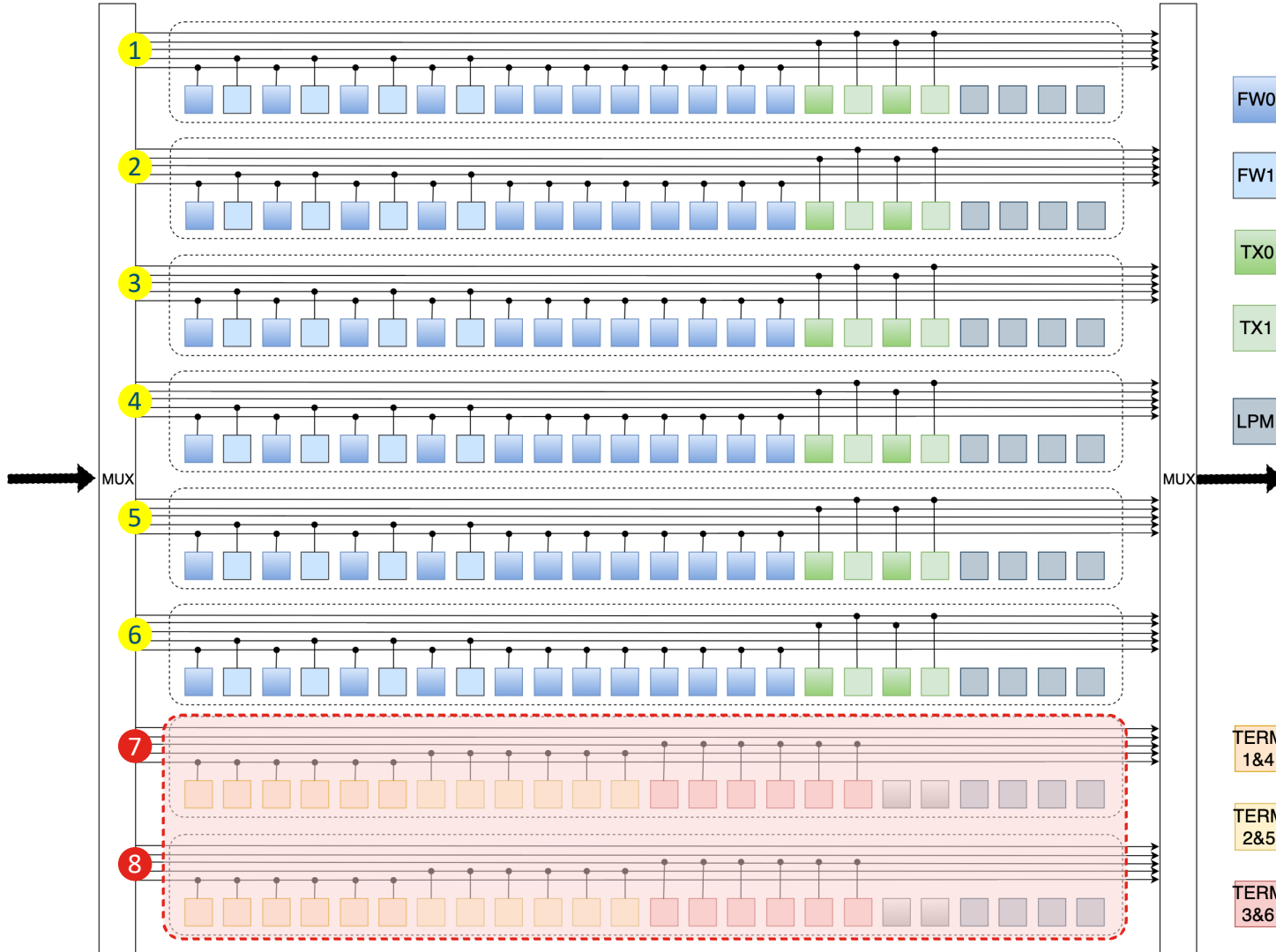
S1 Q200 – ACL Run-Time Flexibility (RTF)

- RTF allows **Security & QOS** (and others), **IPv4 & IPv6**, to share ACL key-fields within the same TCAM space
- Support for RTF for **Ingress ACL only** (API for egress, as well)
- **Multiple ACL Stages** - **input-port** (outer MAC\IP), **pre-forwarding** (on forwarding header), **pre-resolution** and **rx-end**



Catalyst 9500X – ACL TCAM (CDB) Architecture

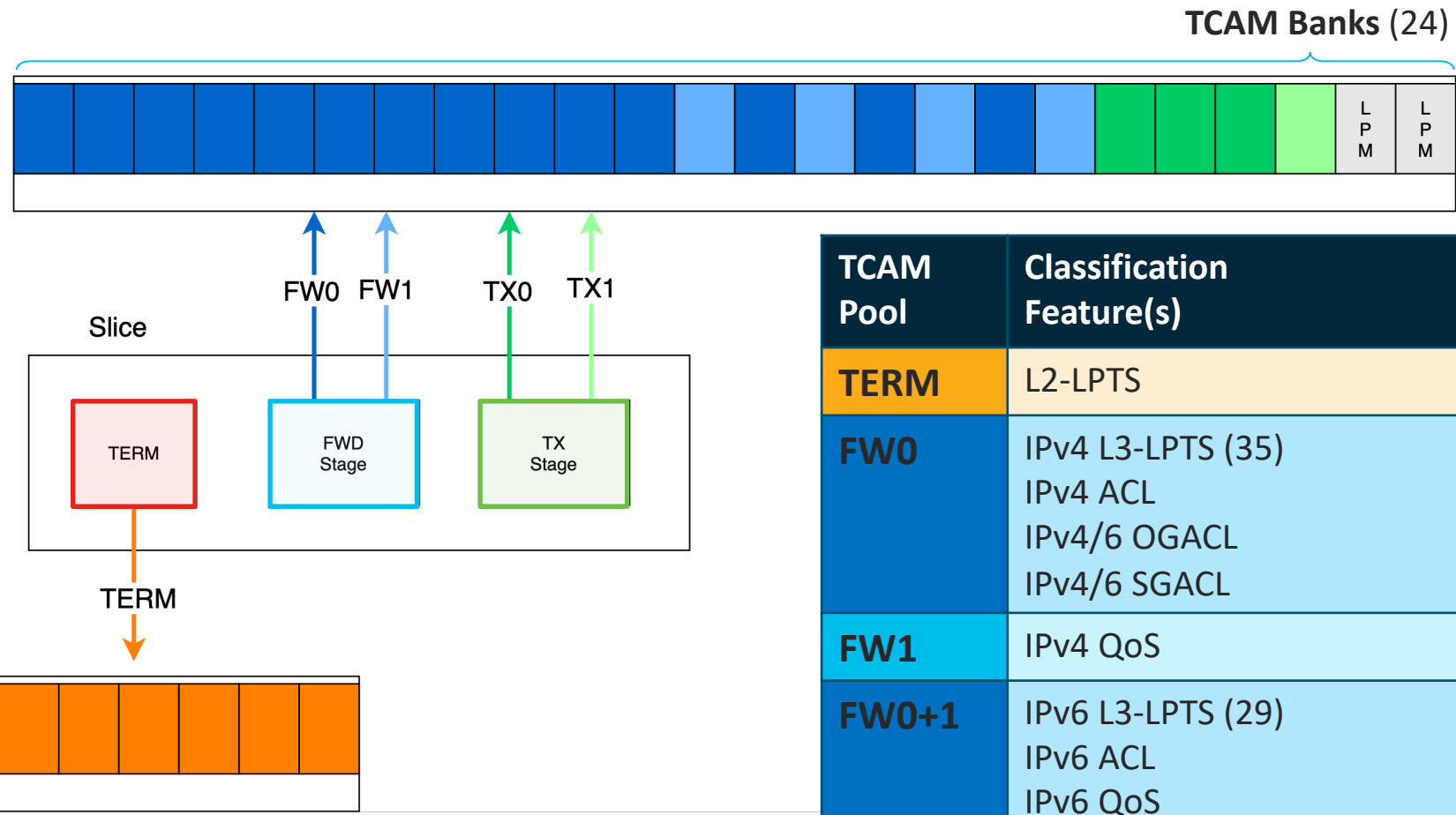
1 TCAM Ring per Slice



- Central TCAM is 8 TCAM rings
 - 24 TCAM banks per ring
 - $8 \times 24 \times 512$ entries = 96K
- 5 inputs per TCAM lookup process
 - 1 TRM + 2 FWD^(RX) + 2 ENC^(TX)
- FWD^(RX) & ENC^(TX) given to 6 slices
 - Single ring per slice ⁽¹⁻⁶⁾
 - each bank accepts 1 input
 - $6 \times 24 \times 512$ = 72K
- TRM uses the remaining 2 rings ⁽⁷⁻⁸⁾
- LPM takes 2-4 TCAM banks (per ring)
 - 20-22 banks remaining
- 512 x 160b per TCAM bank
 - 512×20 = ~10K (L2/IPv4)
- 512 x 320b per TCAM bank-pair
 - $512 \times 20/2$ = ~5K (IPv6)



S1 Q200 - TCAM NPL Access

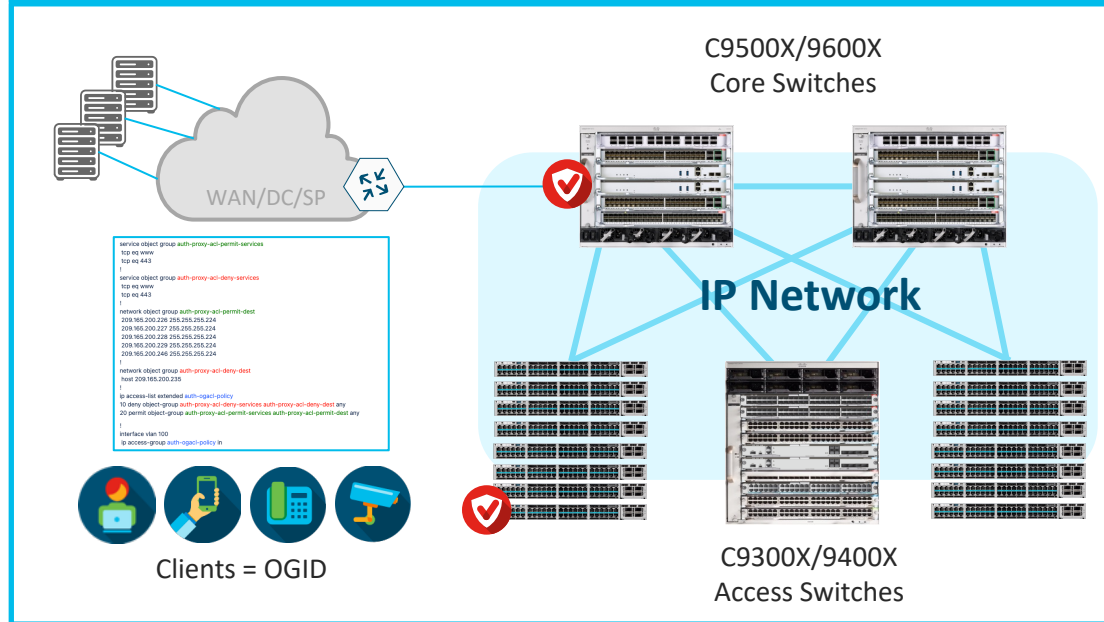


TCAM Pool	Classification Feature(s)
TERM	L2-LPTS
FW0	IPv4 L3-LPTS (35) IPv4 ACL IPv4/6 OGACL IPv4/6 SGACL
FW1	IPv4 QoS
FW0+1	IPv6 L3-LPTS (29) IPv6 ACL IPv6 QoS
TX0	IPv4 ACL
TX0+1	IPv6 ACL

- Key-Size 160b or 320b
- Forward (0+1) stage is large (18 banks)
- Transmit (0+1) stage is small (4 banks)
- Run To Completion – No hardware merge
- Multiple TCAM access impacts PPS
- Limited key-size requires per-feature access
- SGACL is ingress feature

Why OGACL/SGACL in Campus Core?

Object-Group ACLs for IP



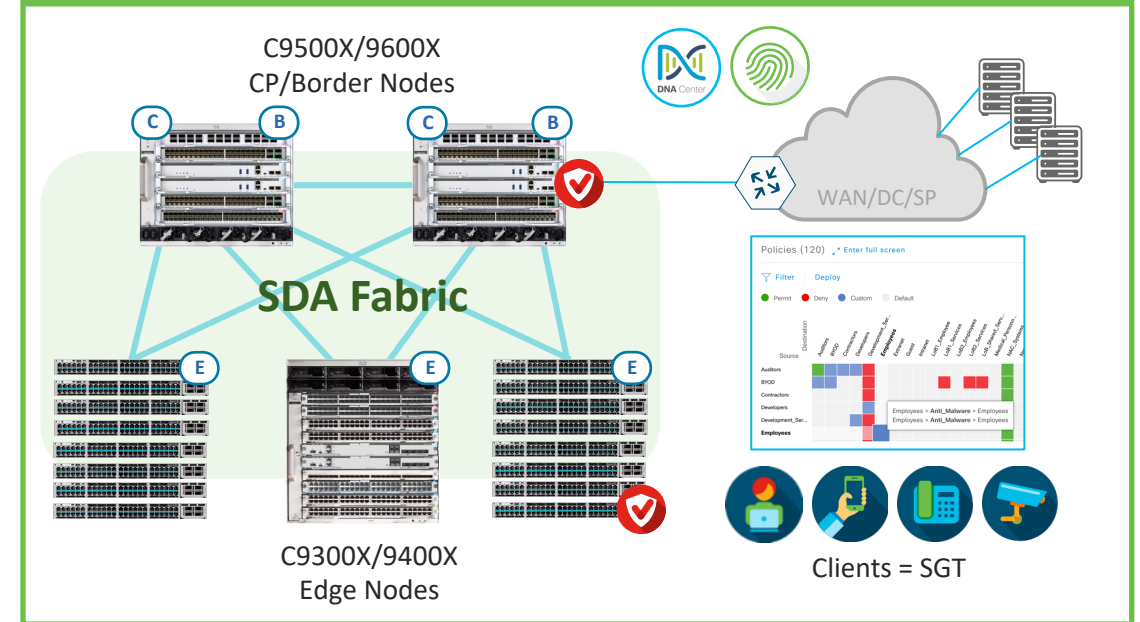
Object-Groups map IP/mask to Labels in CEM

- User defines IP/masks to simple OG name
- OGID labels are stored in Exact Match table

OGACL ACEs take minimal space in ACL TCAM

- Only the Permit/Deny ACEs in TCAM
- OGACLs with same ACEs can reuse entries

Scalable-Groups for SDA



Scalable-Groups map IP/mask to Labels in CEM

- ISE/DNAC defines IP/masks to simple SG name
- SGT labels are stored in Exact Match table

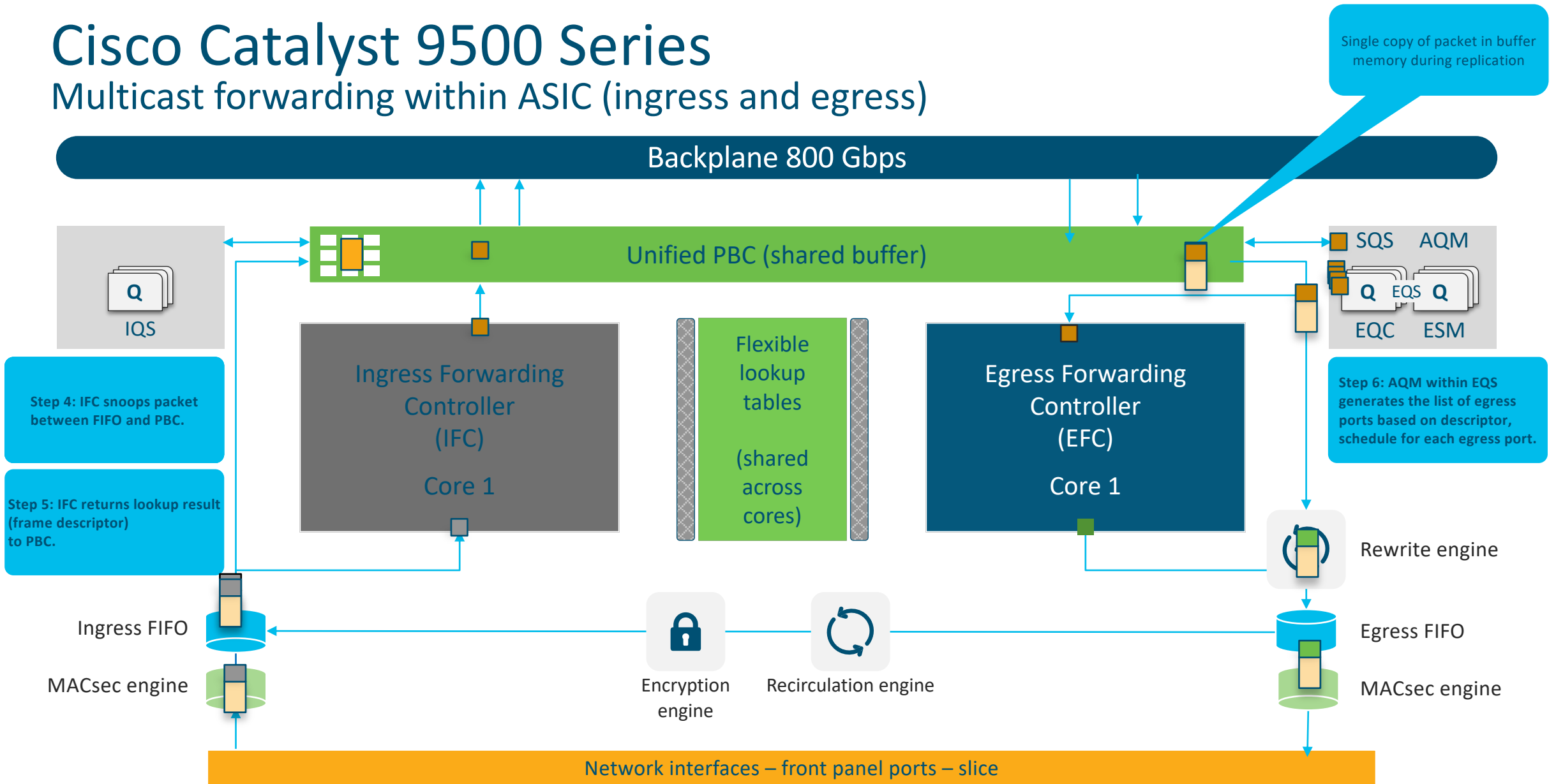
SGACL ACEs take minimal space in ACL TCAM

- Only the Permit/Deny ACEs in TCAM
- SGACLs with same ACEs can reuse entries

Multicast

Cisco Catalyst 9500 Series

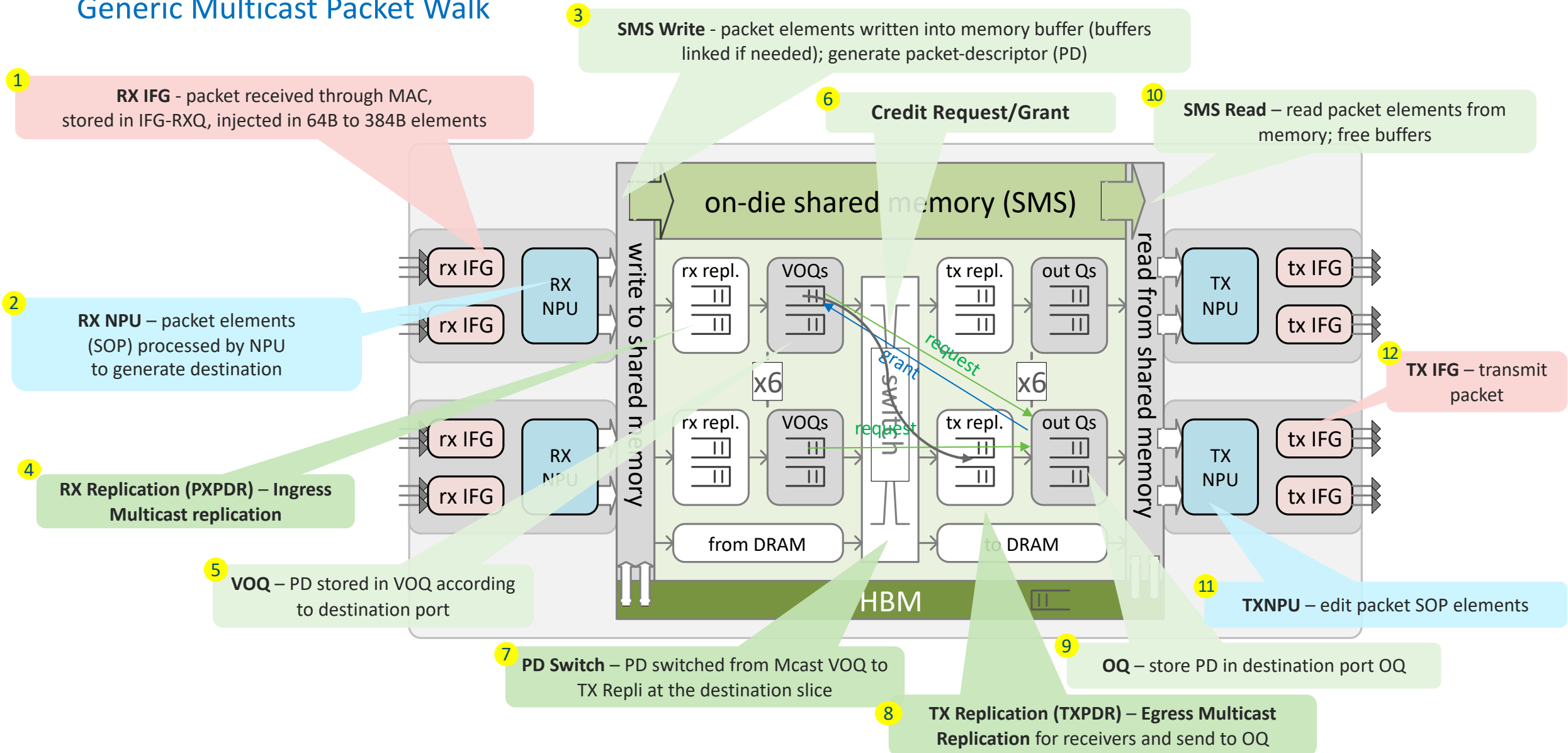
Multicast forwarding within ASIC (ingress and egress)





S1 Q200 - Standalone SOC Architecture

Generic Multicast Packet Walk



Cisco Catalyst 9500 Series – IPv4 and IPv6 multicast

IPv4 multicast

- Multicast Source Discovery Protocol (MSDP)
- IPv4 Auto-RP, BSR RP
- PIM-SM, SSM, and Bidir-PIM
- IPv4 multicast HA
- Multicast VRF-Lite
- Multicast load splitting

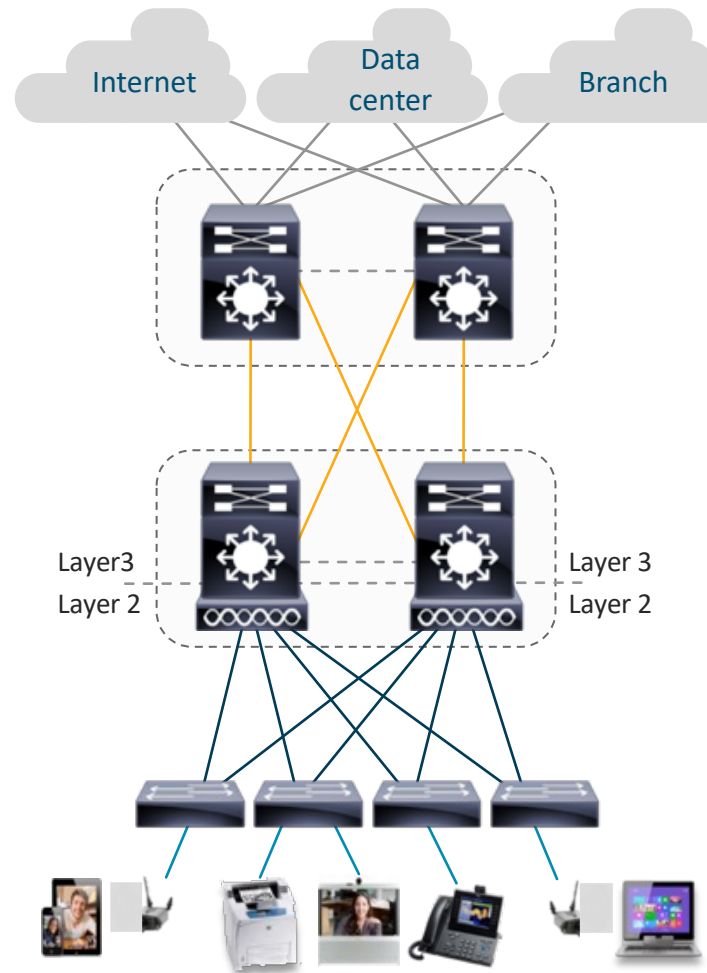
Core

- Dual-stack IPv4/ Pv6
- PIM-SM, SSM, and Bidir-PIM
- IGMP v2,v3 and PIM snooping
- IGMP throttling
- Stub IP multicast routing
- PIM BFD
- IPv4 multicast HA

Distribution

- IGMP v1, v2, v3 and PIM snooping
- IPv4 multicast QoS and ACL
- IGMP v1, v2 filtering

Access



IPv6 multicast

- IPv6 BSR RP
- PIM-SM, SSM, and Bidir-PIM
- IPv6 embedded RP
- IPv6 multicast HA

Core

- Dual-stack IPv4/IPv6
- PIM-SM, SSM, and Bidir-PIM
- Multicast Listener Discovery (MLD) v1, v2 and PIM snooping
- Hardware register and RPF
- HSRP-aware PIM
- IPv6 multicast HA

Distribution

- MLD v1, v2 and PIM snooping
- IPv6 multicast QoS and ACL

Access

Catalyst 9000 Design Consideration

C9600 - Place In Network (PIN)

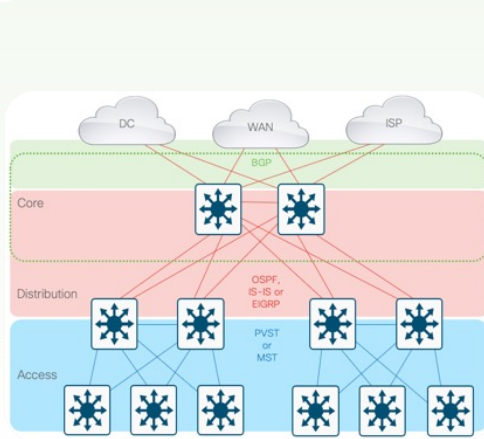
BGP

IGP

STP

1

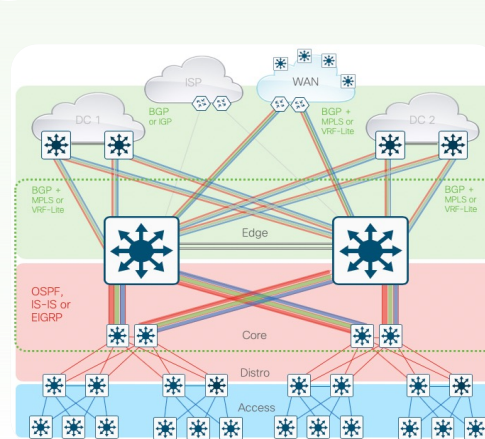
Layer 3 Core



- **Base L3 Routing**
- High-BW, Port Density
- Simple ACL
- Simple QoS

2

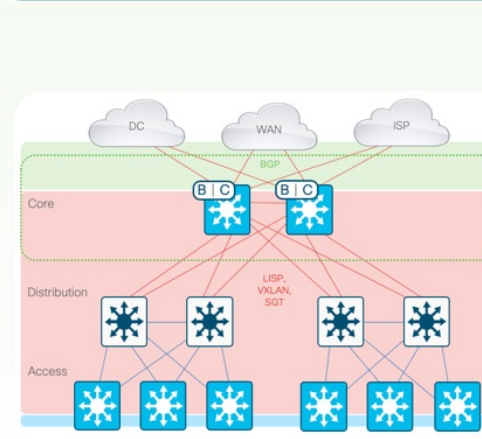
Layer 3 Core + Edge



- **L3 Core + Edge Services**
- DCI, WAN, Internet
- Edge Security, VPN & OGACL
- Complex H-QoS

3

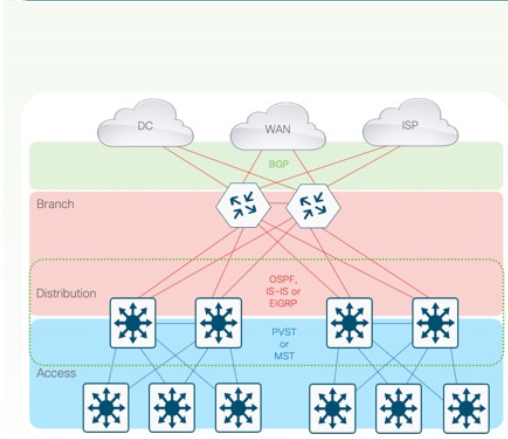
Fabric (SDA & EVPN)



- **L3 Core + VXLAN Fabric**
- Border, Edge, CP/RR
- L2 & L3 VNI & SGACL
- App-based QoS

4

Collapsed Core



- **L3 Core + Distribution**
- L2 Services to Access
- First Hop Security
- Access QoS & AVC



Silicon One™
Q200
©Cisco 2020

039

Edge + Core



Catalyst 9600X
with SUP-2



Catalyst 9500X models



Catalyst 9600
SUP-1

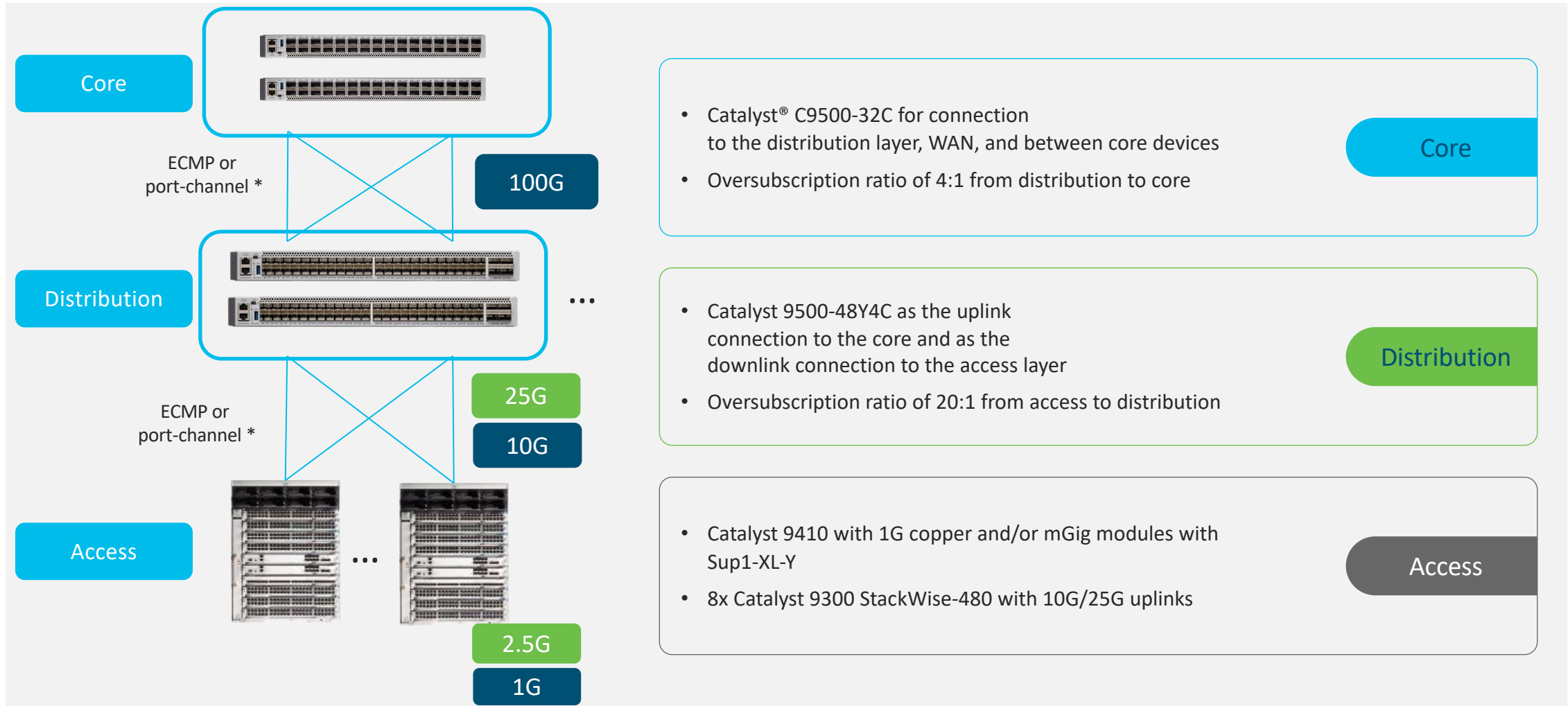


Catalyst 9500
models

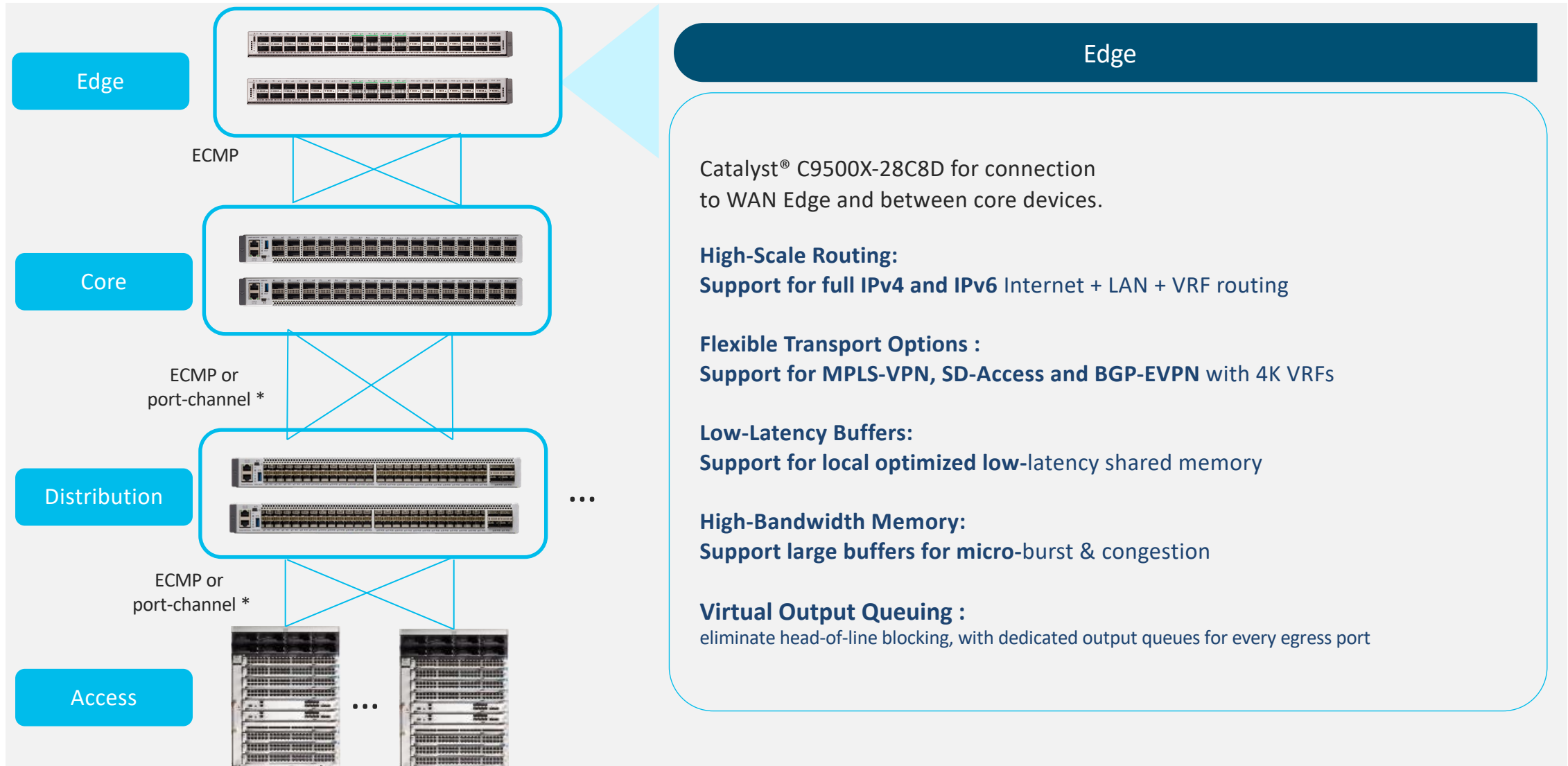
Core + Distribution



Example of a Traditional Three-Tiers Campus Design

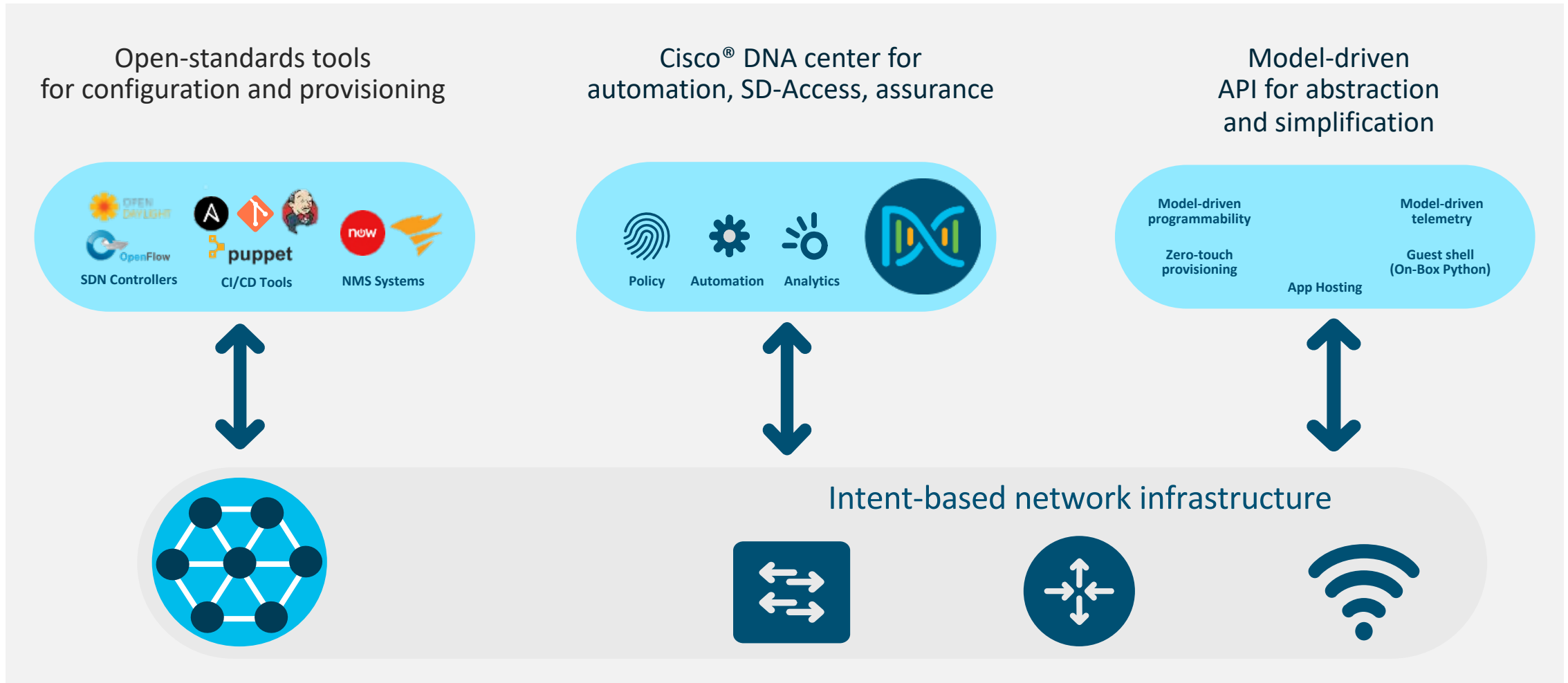


Example of a Four-Tiers - Campus + Edge Design



Intent-based networking

Software Defined – Open, Programmable, Flexible Scaled operations

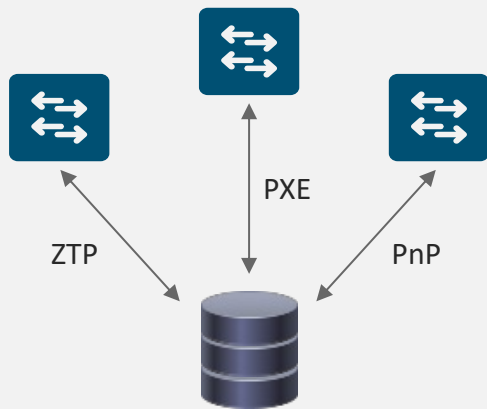


Catalyst 9500 – Simplify network operations open-standards APIs



Day 0

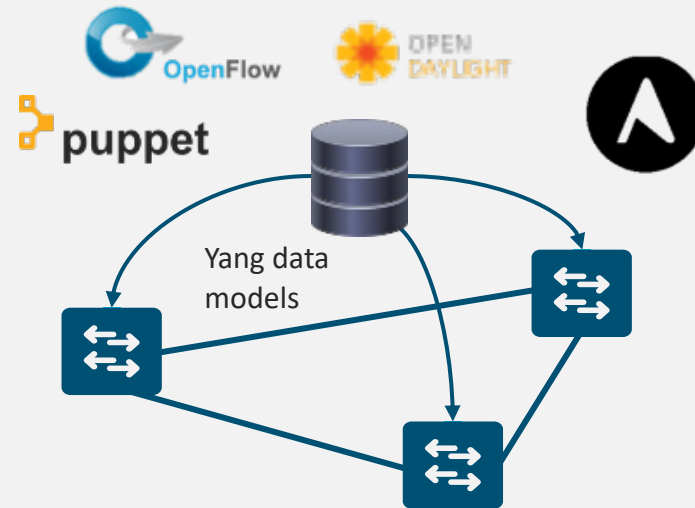
Device onboarding



Automatic device bring-up using industry-standard interface

Day 1

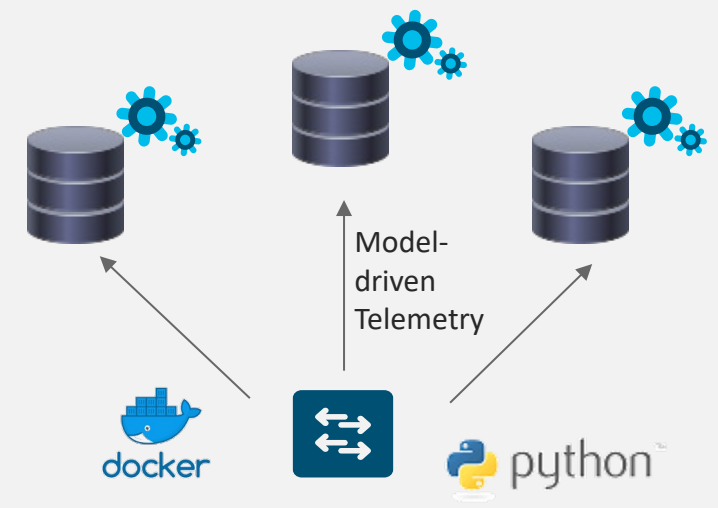
Model-driven configuration mgmt



Open-source tool support for configuration and provisioning

Day N

Monitoring, analytics, SW management

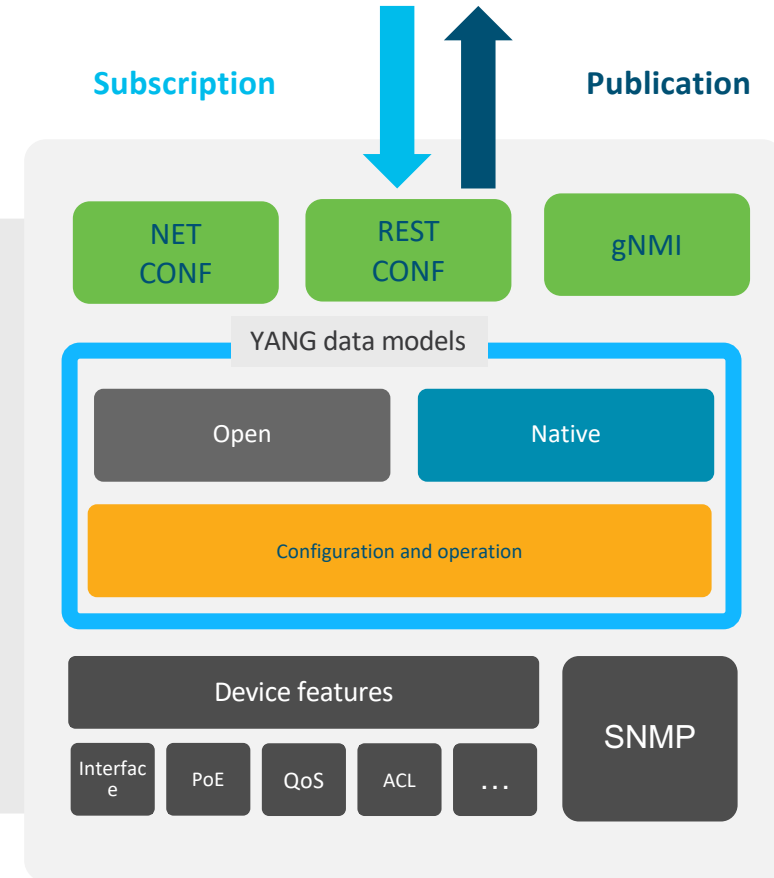


Model-driven telemetry for monitoring and analytics; Docker support for third-party app hosting, On-Box python

Plug in to operational in minutes

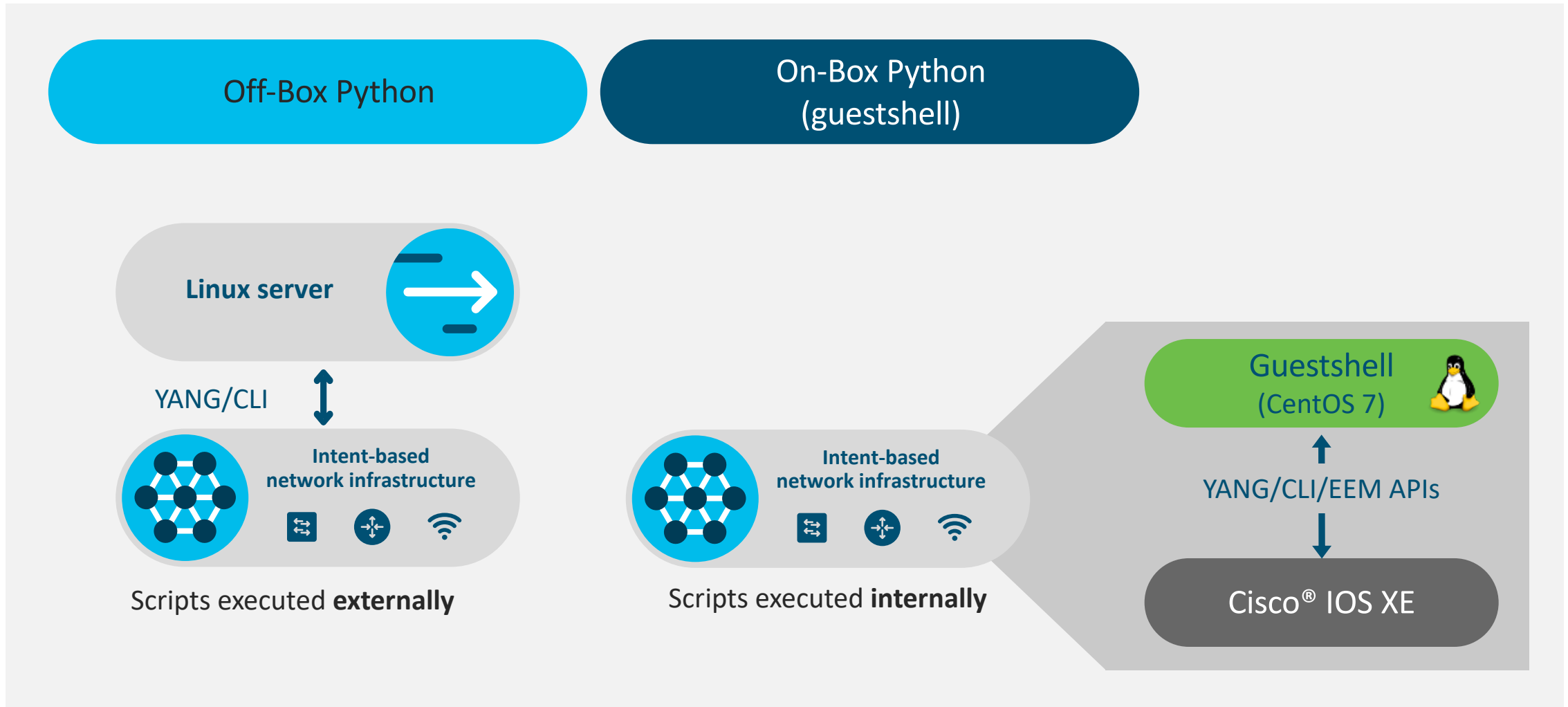
Model-driven telemetry

- Support for any YANG subtree
- Structured data
- XML encoding
- Periodic or on change
- Reduced CPU load



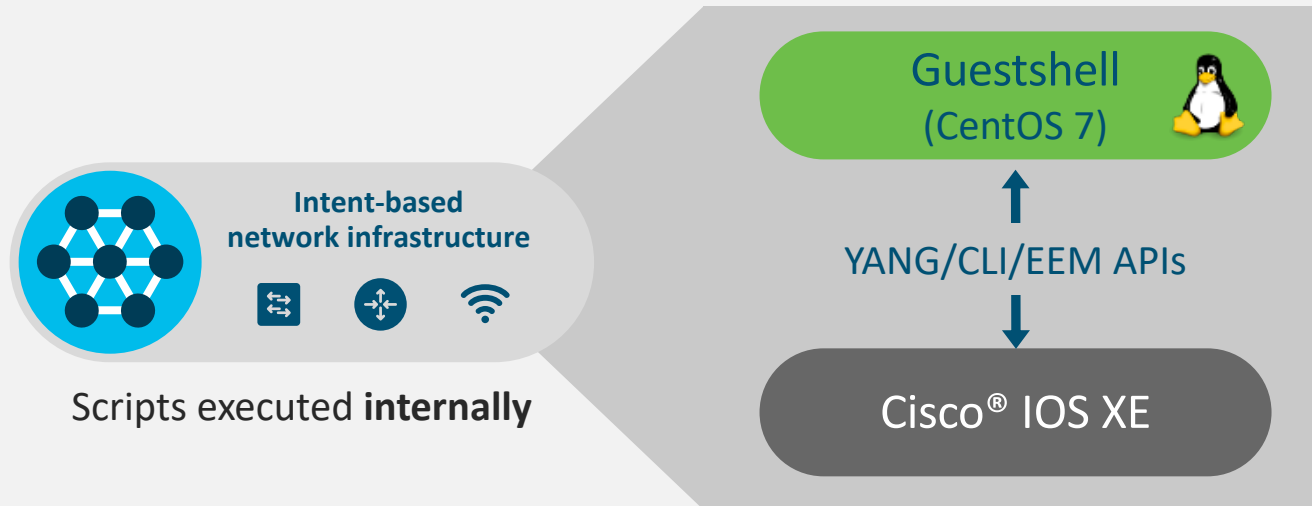
Export enriched, consistent, and concise data with context from devices
for a better user and operator experience

Using Python with Cisco IOS XE devices



Guestshell

- Fault and resource isolation
- Secure Linux shell environment
- Python interpreter
- Integrated with ZTP and EEM
- Disabled by default*
 - `switch# guestshell enable`



Note: Additional config needed from 16.8.1 app-hosting appid guestshell vnic management guest-interface 0

Application hosting on the catalyst 9000

new strategic capabilities for Cisco devices

IT operations and monitoring tools



Consolidate physical infrastructure



IT operations and monitoring tools



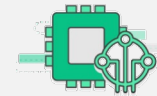
Enhance visibility and security enforcement



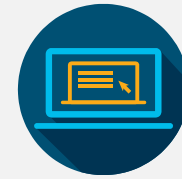
Cloud gateways with serverless edge compute



Reduce app latency and optimize app traffic



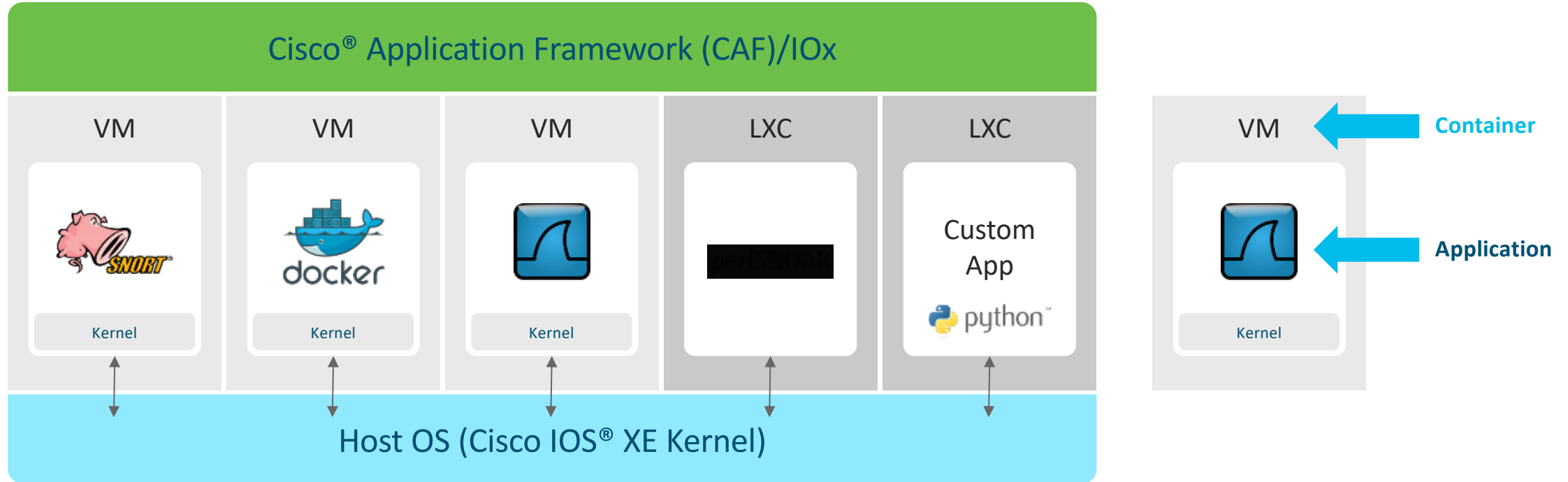
Customer Specific Applications



Derive new insights and respond



Application hosting in the enterprise and IoT



Cisco Catalyst® 9000

Closing



Catalyst 9500X – things to know

Next-generation core + edge switching with Silicon One Q200

C9500X-28C8D



Technology	Brief description	Differences from UADP 3.0
✔ Large LPM table	- Up to 2 million IPv4 or 1 million IPv6 (hash efficiency is about 80%). - Dedicated memory for LPM.	- Up to 256,000 IPv4/IPv6 with custom SDM template. - LPM and other features share 416K ASIC memory.
✔ Large MAC table	- Up to 256,000 MAC entries, custom SDM template. - Shared with other features.	- Up to 128,000 MAC entries with custom SDM template. - MAC shared with LPM, etc. in same 416K ASIC memory.
✔ VOQ QoS + HBM	- Q200 has 80 MB local (low latency) + 8 GB HBM (high-bandwidth memory) buffer memory. - Q200 uses a virtual output queue (VOQ) architecture. All queuing and policing policies applied on ingress.	- Max 36 MB unified buffer memory per ASIC. - Supports both ingress and egress queuing and policing.
✔ OGACL and SGACL	8000 IPv4, 4000 IPv6 ACL TCAM entries. - Object group and security group ACLs use CEM to map IP to group label, TCAM uses only Layer 4 ACEs. (OG/SG ACL design is optimal for Layer 3 environment.)	64,000 ACL TCAM entries per ASIC. - Object group ACLs expand into the TCAM space.
✔ LAN and WAN MACsec*	- Q200 does not have built-in crypto engine - Catalyst® 9500X and 9600X-LC use new CDR5M PHY (400 Gbps full duplex). CDR5M provides line-rate (8x 400G = 3.2T) 802.1ae (LAN) MACsec and WAN MACsec.	- UADP3 has built-in MACsec crypto (speed of ASIC). - UADP3 supports only LAN MACsec (no WAN MACsec).
✔ Flexible NetFlow*	- Q200 does not have built-in flow cache memory (no hardware-based NetFlow). - Catalyst 9500X and 9600X use new software-based Flexible NetFlow (FNF) (≤ 2 million entries), with a dedicated CPU core (~2 Mpps). FNF sampler rate 1:1000, ~10 Tbps of 512-byte packets = ~2 Mpps.	- UADP3 has built-in (hardware) FNF, max 64,000 entries per ASIC. - FNF is shared with LPM, etc., in same 416K ASIC memory.

* Roadmap. Target is Release 17.8.1.

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Next-generation core + edge switching with Silicon One Q200



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- Low speeds (1G to 40G) and port density
- Comprehensive MPLS, EVPN, and SD-Access
- Ideal for campus core, collapsed core + aggregation

**Ideal for Catalyst 6000 Series non-XL
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C9500X-28C8D

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